POLY 88 MICROCOMPUTER SYSTEMS

VOLUME I: ASSEMBLY, TEST, AND THEORY OF HARDWARE

PLEASE NOTE

Errata are included at the end of this manual. Read the Errata pertinent to Volume 1 prior to assembly of any part of your PolyMorphic Systems Package.

TABLE OF CONTENTS

POLY 88 Microcomputer System Manual
VOLUME I: Assembly, Test, and Theory of Hardware

This volume explains how to assemble and test the POLY 88, a complete microcomputer system that interfaces with an ASCII keyboard and video monitor. It also explains how the hardware works. Volume II discusses system software, and offers hands-on experience with the system.

The assembly and test portion of this volume is intended for those who have unassembled kits. If your POLY 88 is assembled, turn directly to Section A.5, system checkout. That section concerns inserting assembled circuit cards into the chassis and checking for correct operation. Those with assembled systems will find the remainder of this volume interesting mainly as a source of reference.

A. Assembly and Test

1. Check all components for inclusion.

The POLY 88 microcomputer system in unassembled form consists of three packages containing the components for the three sub-assemblies, plus a two-volume manual. The three sub-assemblies are:

a. backplane, cabinet, and power supply.
b. central processor sub-assembly.
c. video terminal interface.

Following are complete parts lists. Check each sub-assembly for inclusion of all components. If any component is missing, see the enclosed warranty.

a. Backplane, cabinet, and power supply.

Backplane and power supply components are packed inside the cabinet. Lift off the cabinet and verify that packed inside it are:

check
( ) backplane circuit board
( ) two boxes of components

The cube-shaped box contains the transformer. The other box contains all the miscellaneous components for the backplane and power supply. They are:

check
( ) 1 line cord
( ) 1 17,000 µF capacitor (15V)
( ) 1 2,000 µF capacitor (50V)
( ) 1 1,000 µF capacitor (50V)
( ) 2 100-pin edge connectors
( ) 1 lighted reset button
( ) 1 lighted power switch
( ) 1 fuseholder with hex nut
( ) 2 plastic slotted card guides
( ) 1 strain relief
( ) 1 3-lug terminal strip
( ) 2 6-amp power diodes (60S05)
( ) 4 1-amp power diodes (IN4003)
( ) 1 330-ohm ½ W resistor
( ) 1 0.1 µF ceramic disc capacitor @16V
( ) 2 100-ohm ¼ W resistors
( ) 2 2200-ohm ¼ W resistors
( ) 1 1000-ohm ¼ W resistor
( ) 1 470-ohm ¼ W resistor
( ) 1 2N5449 transistor
( ) 1 1N4148 diode
( ) 6 hexagonal metal standoffs
( ) 2 0.01 µF ceramic disc capacitors @IKV

( ) 2 Card guide brackets (one front and one back)
( ) 4 10-32 screws, lockwashers, and nuts
( ) 24 6-32 X ¼" screws
( ) 4 6-32 X ½ screws
( ) 8 6-32 nuts and starwashers
( ) 4 rubber feet
( ) 2 flat plastic insulators (or plastic backing on brackets)
( ) 2 pairs of Molex connectors with assorted pins
( ) Green, orange, and blue wire (26")
( ) 1 length of shrink tubing
( ) 8 small forked standoffs
( ) 1 2 Amp fuse
( ) solder
( ) black wire (6")
( ) Additional edge connectors, if ordered, plus additional 4-40 screws, nuts, and fiber washers, are also in this box.

b. Processor board

Processor and video board components are packed in the remaining two boxes. The processor board box contains clear plastic bags. One bag contains the processor circuit board. The others, numbered starting with Ø, contain the components to be mounted on the board. Check each bag to see if all components are included.

( ) 1 035020-4-0 Monitor read-only memory

BAG Ø: INTEGRATED CIRCUITS (38 in all)

check
( ) 1 C8080A central processing unit
( ) 1 8224 clock generator
( ) 4 AM91L11APC 256 X 4 random-access memories (or 2111AL-4)
( ) 6 8T97 or 8T95 bus drivers
( ) 3 74LS109
( ) 2 74LS138
( ) 2 74LS174
( ) 2 74LS257
( ) 2 74LS32

( ) 1 74LS08

( ) 1 74LS132

( ) 1 7425

( ) 1 7407

( ) 1 74148

( ) 1 74LS00

( ) 1 74LS02

( ) 1 74LS04

( ) 1 74LS13

( ) 1 40 pin socket

( ) 3 24 pin socket

BAG #1: HARDWARE

check

( ) 2 6107-14 Thermalloy heatsinks

( ) 1 6051 Thermalloy heatsink

( ) 1 mica insulator

( ) 1 LM309K or LM340K-5.0

( ) 1 MC78M12PC

( ) 1 MC79M05PC

( ) 1 Bag hardware

HARDWARE (SHIPPED IN BAG #1)

check

( ) 3 6-32 X3/8" screws

( ) 3 #6 star washers

( ) 4 6-32 hex nuts

( ) 1 #6 fiber washer

( ) 1 6-32 X 3/8" nylon screw

BAG #2: DISCRETE COMPONENTS

check

( ) 24 2,200-ohm resistors

( ) 3 1,000-ohm resistors

( ) 1 4,700-ohm resistor

( ) 8 10,000-ohm resistors

( ) 1 470 pF ceramic disc capacitor
( ) 6 10 μF tantalum capacitors
( ) 1 33 μF tantalum capacitor
( ) 1 39 pF ceramic disc capacitor
( ) 31 0.1 μF ceramic disc capacitors
( ) 2 IN4148 diodes
( ) 1 16.5888 MHZ crystal
( ) 5" teflon sleeving
( ) 6" bare wire

The following bags contain components for options that may or may not have been ordered.

BAG #3: SOCKET KIT

check
( ) 4 18-pin sockets
( ) 17 16-pin sockets
( ) 12 14-pin sockets

BAG #4: RECEIVER/TRANSMITTER PACKAGE

check
( ) 1 MM5307 programmable baud-rate generators
( ) 1 8251 universal synchronous/asynchronous receiver/ transmitter
( ) 1 74LS08
( ) 2 14-pin sockets
( ) 1 28-pin socket
( ) 1 IN4148 diode
( ) 1 79L12 regulator
( ) 1 10 μF tantalum capacitor
( ) 2 .1 μF ceramic disc capacitors

c. Video board

The last box contains bags of components for the video terminal interface. One unnumbered bag contains the circuit board. Check the others for completeness.

BAG #2: HARDWARE, ETC.

check		
( )	30	Capacitor ceramic .1mf @ 16V UK16-104
( )	1	Heat sink 6051
( )	14	Resistor 2200 ohm ¼w
( )	1	Bag Hardware

VIDEO HARDWARE (SHIPPED IN BAG #2)

check		
( )	2	6-32 x 3/8" pan head screws
( )	2	#6 Hex nut (small pattern)
( )	2	#6 Lockwasher
( )	1	6" #24 bare wire
( )	1	6" Teflon sleeving
( )	1	15 feet solder

BAG #3: MEMORY OPTION

check		
( )	4	Capacitor Ceramic .1mf @ 16v
( )	4	AM91L11APC or 2111AL-4

BAG #4: SOCKET SET

check		
( )	2	Crimpable contact
( )	1	Male 2 pin connector
( )	1	Plug Housing
( )	11	Socket-14 pin
( )	18	Socket-16 pin
( )	8	Socket-18 pin
( )	1	Socket-20 pin
( )	4	Socket-24 pin
( )	1	14 pin sidewiping
( )	1	14 pin DIP Slide Switch

BAG #5: POLY 88 ACCESSORIES

check		
( )	1	HARDWARE FOR 25 PIN CONNECTOR
( )	1	25-PIN CONNECTOR
( )	1	REAR MTG PHONO PLUG
( )	1	RIBBON CABLE
( )	1	PC BOARD-PARALLEL
( )	1	BAG HARDWARE
( )	1	COAXIAL CABLE 1 FOOT

HARDWARE (SHIPPED IN BAG #5)

check		
( )	2	4-40 x 3/8" Screws
( )	2	4-40 Hex nuts
( )	2	#4 Star washers
( )	1	1" shrink tubing
( )	1	6" #22 AWG stranded wire

2. Assemble cabinet, backplane, and power supply

The first step in building the POLY 88 is assembling the backplane, starting with the discrete electronic components (smallest through largest), then card guides., then sockets. The transformer is then assembled into the chassis, and the backplane mounted and connected.

a. Assemble backplane. Refer to figure A-1 to see where the components go on the board. When installing discrete components, solder on the back of the board and trim leads.

( ) 1. Install the IN4148 diode D7.
( ) 2. Install two 2,200-ohm resistors R1 and R2. (red-red-red)
( ) 3. Install one 100-ohm ¼ W resistor R4.
( ) 4. Install the other 100-ohm ¼ W resistor R5.
( ) 5. Install standoffs for four 1-amp power diodes, with forks up. (for De through D6 -- see fig. A-1.) Clip off extra pin below board. NOTE: The extra holes with diode symbol nearest the center are not used.
( ) 6. Install 1A diodes (1N4003) onto standoffs (D3 through D6) oriented as indicated by the arrow on the board. The banded end of the diode points in the direction the arrow is pointing.
( ) 7. Install the 1,000-ohm resistor R6 at the other end of the board. (brn-blk-red).
( ) 8. Install the 470-ohm resistor R7. (ylw-viol-brn)
( ) 9. Install the 2N5449 transistor Q1 oriented as shown.
( ) 10. Install the 330-ohm ½ W resistor R3. (orange-orange-brown)
( ) 11. Install both 6-amp power diodes (D1-D2).
These two diodes alone provide full-wave rectification with the center-center-tapped transformer. (60S05) - mount them up off the surface of the board.
( ) 12. Install the ceramic disc capacitor C4. (.1 μF)
( ) 13. Install the 1,000 μF electrolytic capacitor C2 oriented with its positive end in the direction indicated on the board.

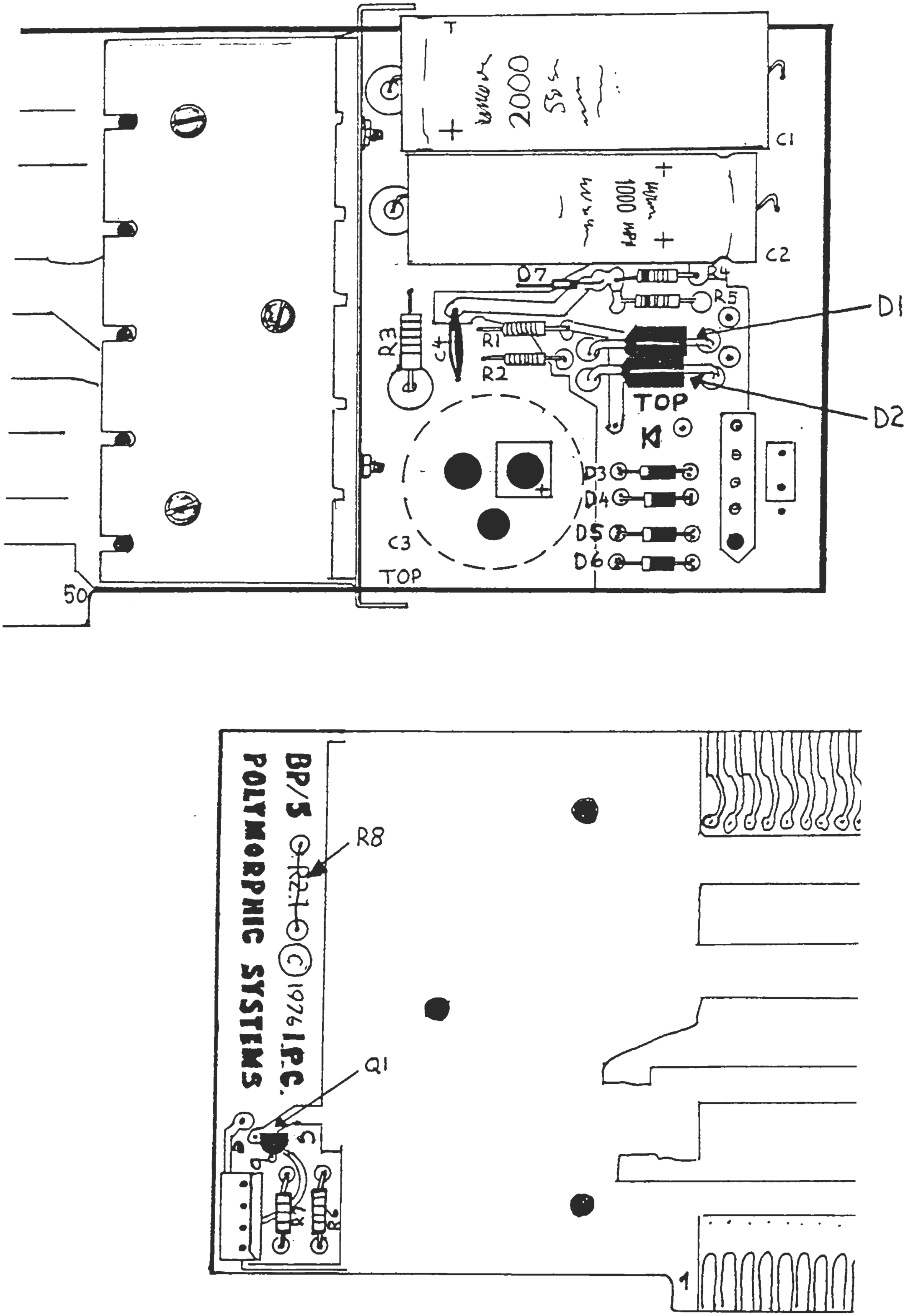

2000
C1
1000
C2
D7
R4
R5
D1
R3
C4
R1
R2
TOP
D2
K1
D3
D4
D5
D6
C3
TOP
50
BP/5
R8
R2.1
© 1976 I.P.C.
POLYMORPHIC SYSTEMS
Q1
c
b
R1
R2
1

Fig. A-1

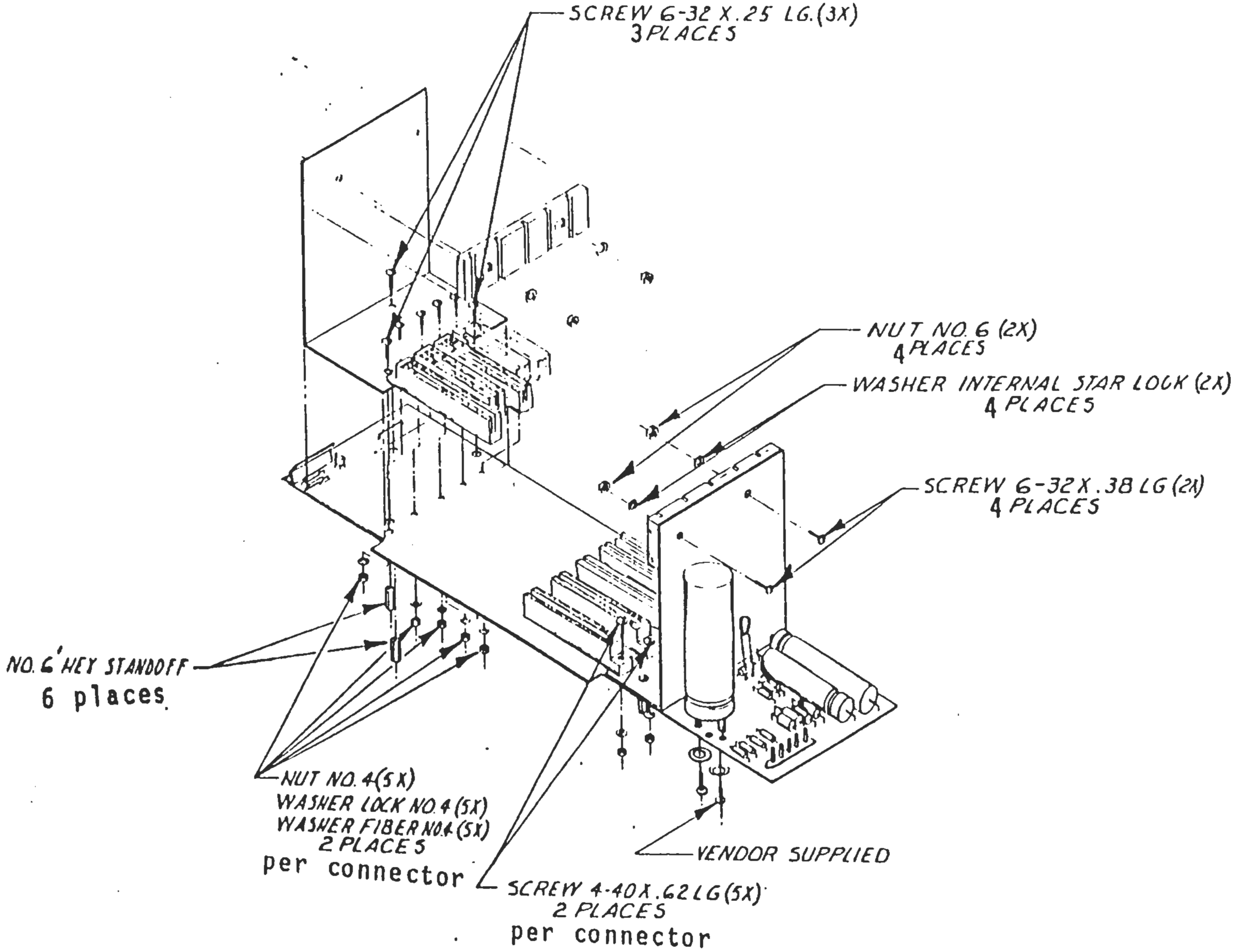

SCREW 6-32 X .25 LG.(3X)
3 PLACES
NUT NO. 6 (2X)
4 PLACES
WASHER INTERNAL STAR LOCK (2X)
4 PLACES
SCREW 6-32 X .38 LG (2X)
4 PLACES
NO. 6 HEX STANDOFF
6 places
NUT NO. 4 (5X)
WASHER LOCK NO. 4 (5X)
WASHER FIBER NO. 4 (5X)
2 PLACES
per connector
SCREW 4-40 X .62 LG (5X)
2 PLACES
per connector
VENDOR SUPPLIED

Figure A-2

( ) 14. Install the 2,000 μF electrolytic capacitor C1, oriented with its positive end in the direction indicated on the board.

( ) 15. Using the screws supplied on the capacitors, attach the 17,000 μF electrolytic capacitor C3. (Noting the polarity)

( ) 16. Attach plastic card guides to metal card-guide supports, using 6-32 screws and nuts. (Nuts on inside.)

( ) 17. Mount card guides as shown. Use short 6-32 screws and six metal standoffs. These are protected from the circuit board by plastic insulators.

( ) 18. Attach two 100-pin edge connectors (or up to five as desired) into connector areas J1 and J5 as shown. Making sure that the connector does not bow the backplane, solder all 100 pins on each connector. Be careful not make solder bridges.

( ) 19. Solder male halves of Molex connectors into each end of board as shown on page 10.

( ) 20. Install a wire jumper on front of board as shown. (R8)

The backplane is now complete.

b. Assemble chassis.

Do not solder until instructed to do so.

( ) 1. Install 4 rubber feet to chassis undersides, using 4 #6-32 x 3/8 screws, nuts, and lockwashers.

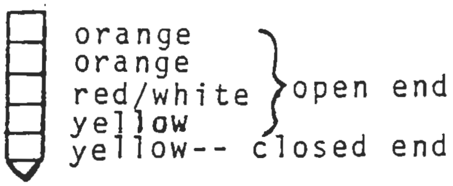
( ) 2. Install fuseholder on rear of chassis, with perpendicular tab pointing down.

( ) 3. Tin the line cord wires and trim the exposed ends to about 3/8".

( ) 4. Install through rear of chassis using the strain relief provided, allowing about 2 inches of the heavy outside insulation inside beyond the strain relief. Pliers or a strain relief tool will be necessary, due to the tight fit.

( ) 5. Attach the black wire from the line cord to the end of the fuseholder and solder in place.

( ) 6. Take the transformer and cut the secondary wires (yellow, orange, red, white) to 7 inches, then strip about 3/8" and tin.



( ) 7. Attach and solder the 5 larger molex pins to secondary wires, making sure the one with the closed tip goes on one of the yellow wires, and the red and white wires are together on one pin. Use needle pliers to crimp pins and solder to insure good connections.

( ) 8. Insert molex pins in the connector as shown above.

( ) 9. Cut the blue and black primary wires down to 5 inches and the red and brown wires to 8½ inches, strip to about 3/8 inch, and tin.

( ) 10. The remaining 2 wires (green, gray) must be kept from shorting to anything else. Cut one of these wires to about 3 inches and the other to 2 3/4 inches, place a 1 inch length of shrink tubing on the two wires so that ¼ inch extends past the end of the longer wire. Shrink the tubing by using a match; pinch the end of the warm tubing to seal the wire inside.

CAUTION: Do not burn the tubing by allowing the flame to touch it.

( ) 11. Install rocker power switch in front of chassis with the 2 closer contacts at the top.

( ) 12. Take the 3 20 inch lengths of wire, strip to about 3/8 inch and tin (both ends). Then twist the 3 wires together, leaving 1½ inch loose at each end.

( ) 13. Attach and solder these 3 wires to the power switch from the bottom up. The order should be green-bottom, orange middle, and blue-top.

( ) 14. Take the 3 lug terminal strip and attach green wire from line cord to the grounded lug on terminal strip and the white wire to another lug. To make later connections to terminal strip lugs easier, it is helpful to attach the line cord wires to the lug rivets on the bakelite strip rather than on the ends of the lugs. If you do this, solder the line cord wires in place now. This terminal strip will be attached to the foot of the transformer as shown on the next page.

( ) 15. Attach 1 of the .01 μF disc capacitors from the side lug of the fuseholder to the terminal strip lug with the green wire attached.

( ) 16. Attach the blue wire from the power switch on the front of the chassis to the side lug on the fuseholder, and solder at this point.

( ) 17. Attach the green wire from the power switch to the same terminal strip lug to which you already attached the white line cord wire.

( ) 18. Attach and solder the remaining .01 μF capacitor between the lug used in step 17 and the grounded lug of the terminal strip and solder the lug with the two caps.

( ) 19. Placing the transformer beside the chassis, but without yet installing it, attach its blue and black primary wires to the term lug with the white line cord wire and solder.

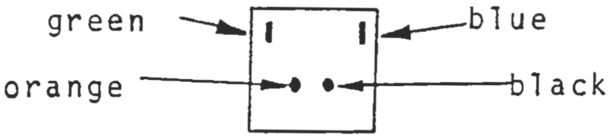
( ) 20. Take the transformer and turn it so the secondary wires are on the same side as the terminal strip and attach it into place in the rear of chassis, being very careful not to pinch any wires under it. The terminal strip should be installed on one foot of the transformer above the fuseholder.

( ) 21. Attach the orange wire from the power switch and remaining red and brown primary wires from the transformer to the remaining empty lug on the terminal strip and solder. These are the only connections to this lug.

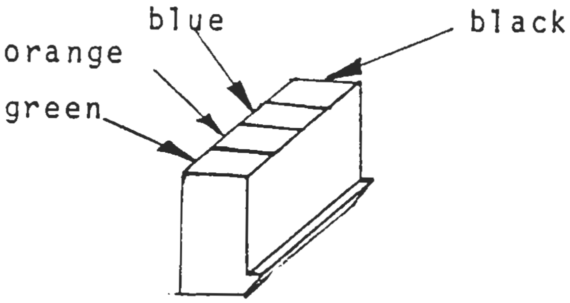
( ) 22. Solder all connections to the terminal strip now.

( ) 23. Take the 4½ inch long wires (orange, black, green, blue), strip and tin both ends to about 3/8 inch, and crimp the 4 smaller molex pins to one end. Solder again to insure good connections.

( ) 24. Trim off about half of the two thin wire pins in the center of the reset button. Attach and solder the 4 wires to the button as shown:



( ) 25. Insert molex pins into the small female molex connector as shown:



( ) 26. Insert connector through square hole on front panel and draw the wires through. With the green and blue wires at the top, snap the switch firmly in place.

( ) 27. Assemble backplane into chassis by sliding the end with the two horizontal filter capacitors under the transformer, align the hexagonal standoffs with the six holes in the bottom of the chassis. Fasten the backplane in place with six #6-32 screws, making sure not to pinch the wires running to the power switch.

( ) 28. Connect the backplane to the transformer and the reset switch by mating the molex connector at each end of the backplane.

The cabinet, backplane, and power supply assembly is now complete.

c. Test backplane and power supply.

If you have a small voltemeter, you can now check the backplane and power supply. Plug in the chassis and "smoke test" it. If anything is obviously wrong, don't go any further till you've eliminated the problem.

Next, turn the cabinet so that the transformer is on your left. Along the edge of the backplane circuit board nearest you is a row of finger-like pads. These are the pads you would solder a connector to, in order to mate this chassis to another. They also make a convenient voltage check point. At each end of this row you will find a pad much wider than the others. The one on the right is ground; attach the ground lead of the voltmeter to this point, being careful not to include the adjacent pad. (The ground pad is available on both upper and lower surfaces of the board.)

CAUTION!

The pad on the left end of the board is next to a minus-voltage pad on the upper surface of the board and a plus-voltage pad on the lower surface. If the upper surface of the board is shorted to the lower, serious damage will result. Do not clip your volt-meter lead to this end of the board. Instead, probe carefully at the indicated pads.

The pad on the left end should read between +8 and +10 VDC. The pad just to its right on the upper surface of the board should have -18 to -22 VDC. The pad on the lower surface next to the large end pad should have +18 to +22 VDC.

3. Assemble Processor Board

The central processor circuit card consists of the Intel 8080A that provides all central processing, plus the devices that support the central processor: random-access and read-only memory, plus optional serial port if ordered.

Orient the board as shown in figure A-3.

a. Install components required for voltage regulation.
1. The following ICs are not dual in-line packages. Each of these ICs has a heat sink.

Check	IC#	Part #	Function
( )	32	7805 or LM309 or LM340K-5.0	5V regulator
( )	33	78M12	12V regulator
NOTE:	Install IC 34 with mica wafer and non-conductive screw.		
( )	34	79M05	-5V regulator
	44	79L12	-12V regulator*

*Include with Serial Option only

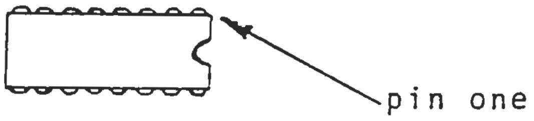
2. Install the following capacitors.

CHECK	CAP. #	TYPE
( )	20	10 μF tantalum
( )	21	0.1 μF ceramic disc
( )	32 through 35	10 μF tantalum
( )	36 and 37	0.1 μF ceramic disc
( )	38	10 μF tantalum

3. Now you can test voltage regulation. ( ) Check pin 28 of IC 14 (CPU) for 12V± 0.6 V. ( ) Check pin 20 for 5V ± 0.25 V. ( ) Check pin 11 for -5V ± 0.25 V. If proper voltages are not present, check the installed components and the solder points. Check continuity between IC 43 (78 M05) and ground (outer trace); if resistance does not exceed 1,000 ohms, check the insulation on this IC. The metal tab should be insulated by the nylon screw and mica washer.

b. Install integrated circuits. Begin by installing the integrated circuits themselves, OR the optional sockets if you bought them.

If you bought the socket option, install and solder in place all sockets by referring to figure A-3 and the list of componenets below. DO NOT install the integrated circuits at this time; install them after completing Step C below. Verify the location of each socket by checking the number of pins. Verify that the orientation is correct by noting the "pin one" location on the figure.



If you did not buy the socket option, install and solder into place all the integrated circuits by referring to the figure and list as above, verifying location and orientation as above.

CHECK	IC#	TYPE	#PINS	FUNCTION
( )	1	74LS13	14	Quad NOR gate
( )	2	74148		Decoder
( )	3 through 8	8197	16	Bus driver
( )	9	7407	14	Hex buffer
( )	10	74LS109	16	
( )	11	74LS02	14	
( )	12	74LS04	14	Hex inverter
( )	13	8224	16	Clock generator
( )	14	Socket	40	Socket for CPU
( )	15 and 16	74LS257	14	
( )	17	74LS174	14	
( )	18	7425	14	
( )	19	74LS08	14	
( )	20	74LS132	16	
( )	21 through 24	91L11	18	256X4 RAM
( )	25 through 27	Sockets	24	Sockets for ROM
* ( )	28	Socket	28	Socket for USART
* ( )	29	MM 5307	16	Baud rate generator
( )	30	74LS174	16	
* ( )	31	74LS08	14	
( )	35 and 36	74LS138	16	
( )	37	74LS32	14	Quad NOR gate
( )	38	74LS109	16	
( )	39	74LS32	14	Quad NOR gate
( )	40	74LS00	14	Quad NAND gate
( )	41	74LS109	16	
* ( )	42 and 43	Sockets	14	Socket for serial post

c. Install discrete components.
Install all resistors, starting at the lower left hand corner of the board.

*Included with Serial option only.

Install Resistors

CHECK	#	TYPE
( )	1 through 11	2,200-ohm
( )	12	4,700-ohm
( )	13	2,200-ohm
( )	14	1,000-ohm
( )	15 through 17	2,200-ohm
( )	18	1,000-ohm
( )	19 through 20	2,200-ohm
( )	21	1,000-ohm
( )	22 through 23	2,200-ohm
( )	24 through 31	10,000-ohm
( )	32 through 36	2,200-ohm

Install all capacitors, starting at the lower left corner.

CHECK	#	TYPE
( )	1 through 7	0.1 µF ceramic disc
( )	8	470 pF ceramic disc
( )	9 through 13	0.1 µF ceramic disc
( )	14	33 µF tantalum
( )	15 through 18	0.1 µF ceramic disc
( )	19	39 pF ceramic disc
( )	22 through 31	0.1 µF ceramic disc C25, C30*
( )	39 through 42	0.1 µF ceramic disc
( )	43	10 µF tantalum*

Install all diodes. The end of the diode with the colored band points in the same direction as the arrow etched on the board.

*Included with Serial option only.

CHECK	#	TYPE
( )	1 and 2	1N4148
( )	3	1N4148*

If you bought the socket option, you can now check voltage regulation without endangering your chips. Install the board into any chassis edge connector (it will not go in wrong) then turn on the power and use a small voltmeter to verify +5V, +12V, -5V, and -12V.

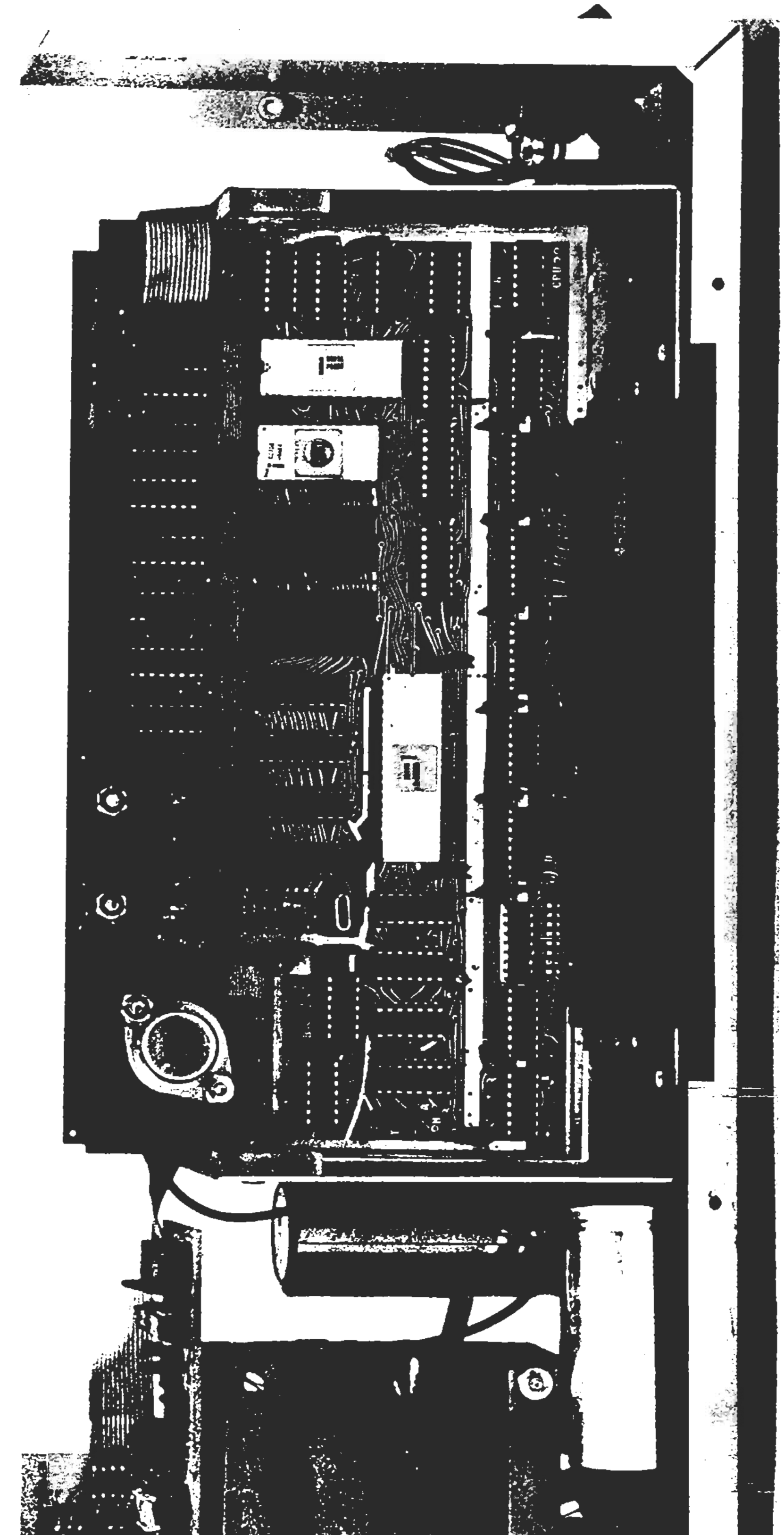
CHECK		
( )	X1	Install 16.5888 MHz crystal

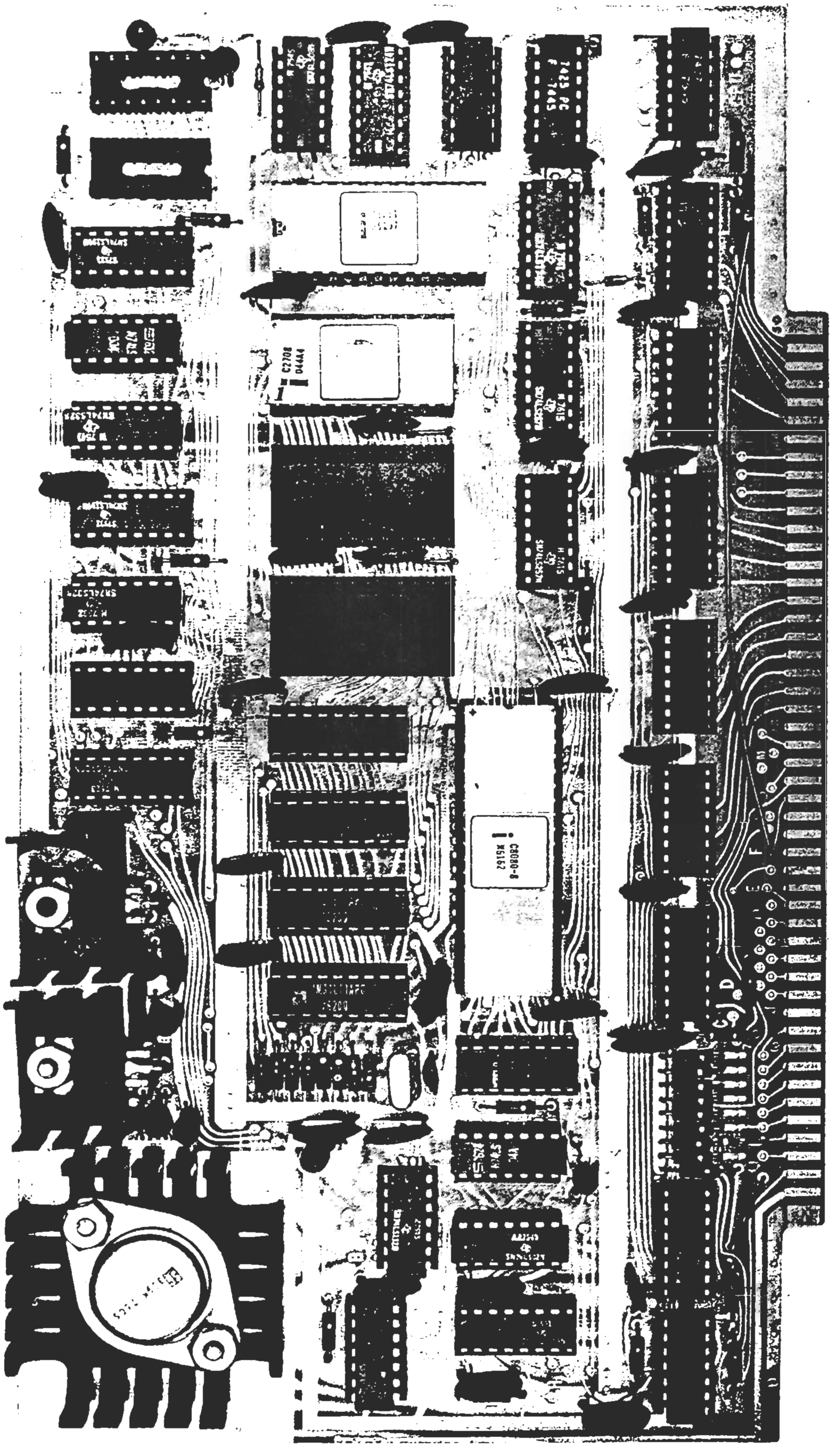
Install jumper using teflon tubing from point labeled "F" near pin 21 on the edge connector to the corresponding point "F" below IC 8.

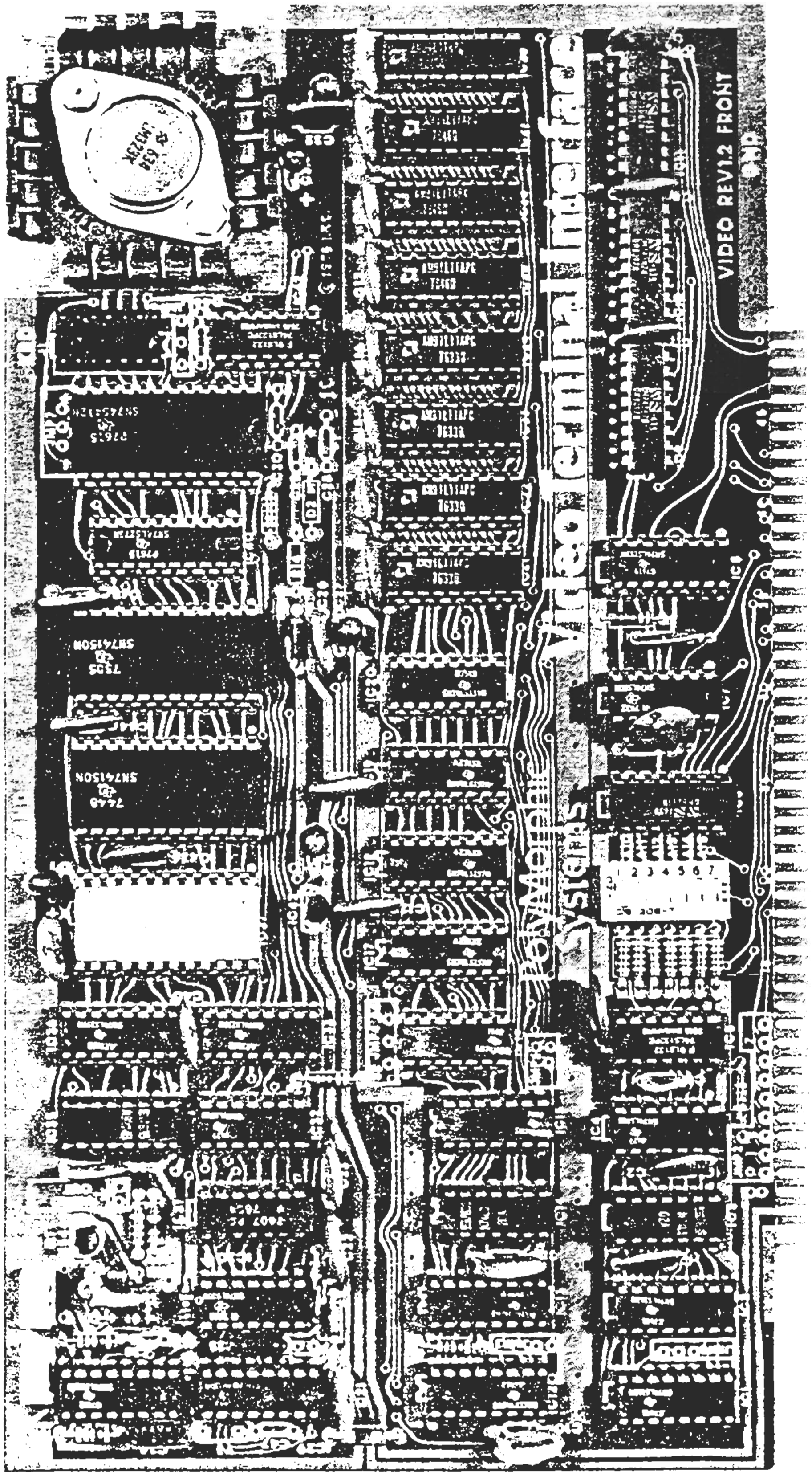
If the power supply checks out, install all ICs now. If power supply is not correct, fix it (check for solder bridges, mis-oriented components, etc.) before installing chips.

The CPU board is now complete.

*Included with Serial option only.




C8080-8
M5162
C2708
D4444


Video Terminal Interface
PolyMorphic Systems
VIDEO REV1.2 FRONT
GND

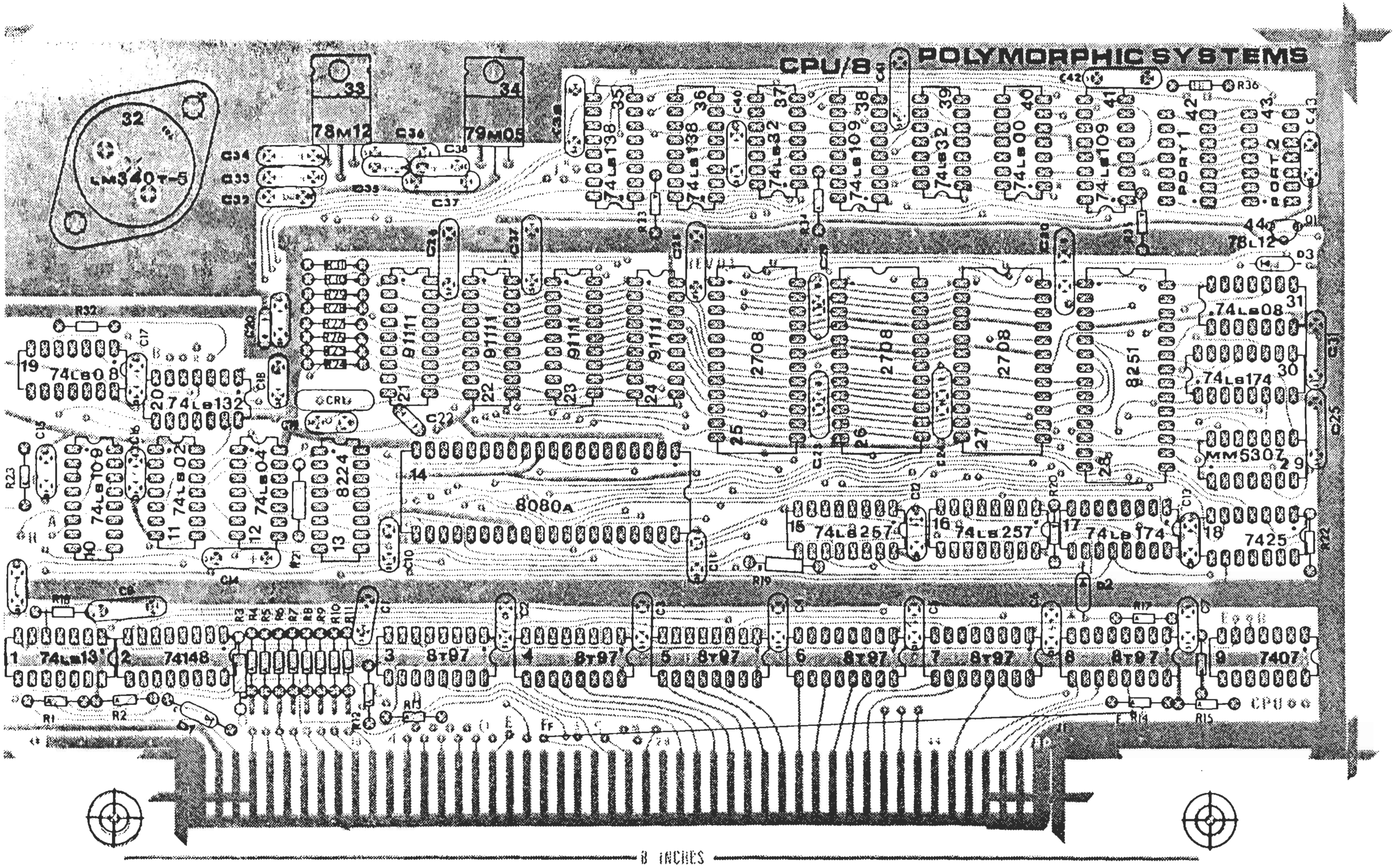
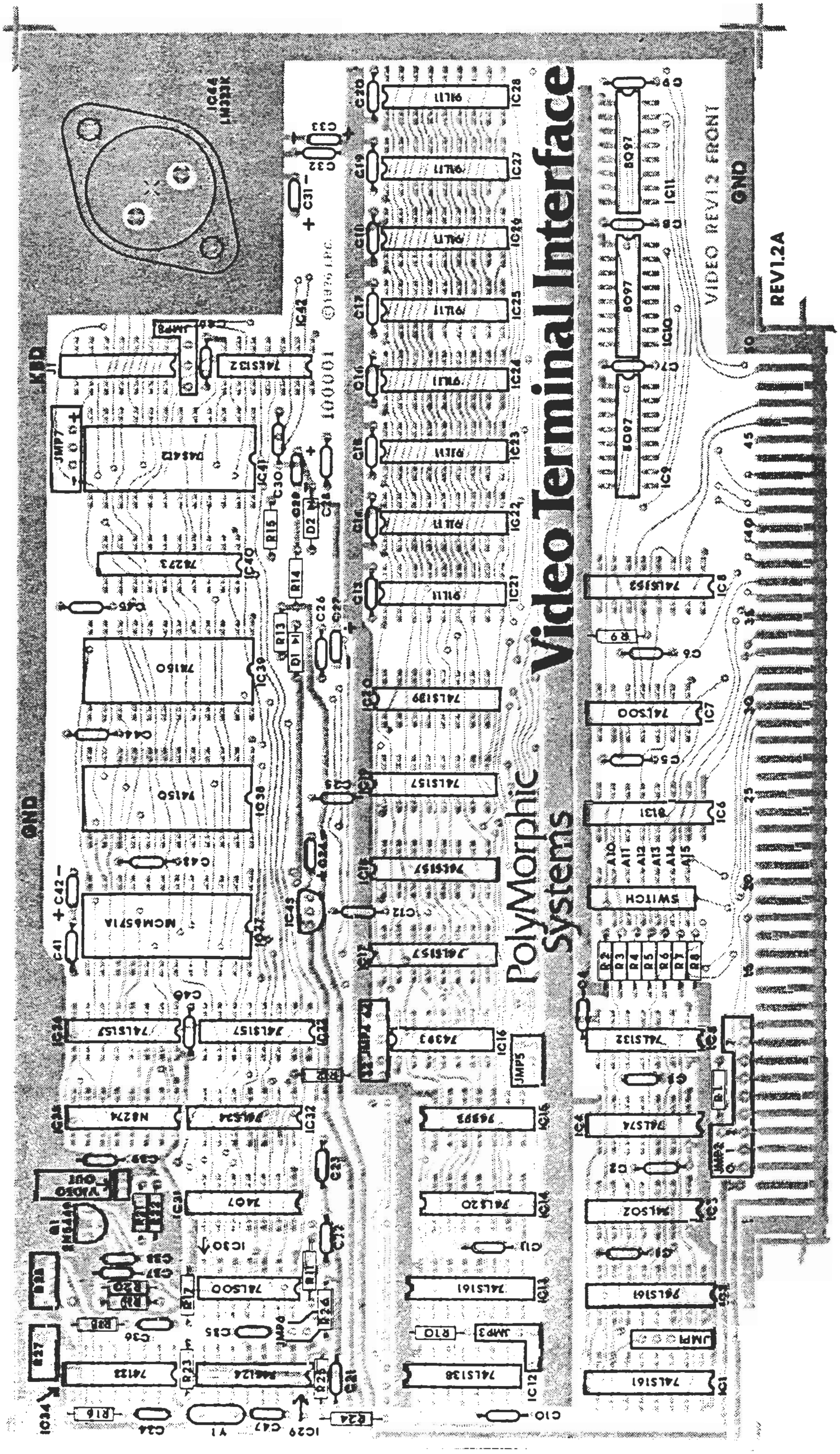

CPU/8
POLYMORPHIC SYSTEMS
32
LM340T-5
33
78M12
34
79M05
C32
C33
C34
C35
C36
C37
C38
C39
C40
C42
C43
R36
35 74LS138
36 74LS138
37 74LS32
38 74LS109
39 74LS32
40 74LS00
41 74LS109
42 PORT 1
43 PORT 2
44 78L12
Q1
D3
R13
R34
R35
31 74LS08
30 74LS174
29 MM5307
28 8251
27 2708
26 2708
25 2708
24 91111
23 91111
22 91111
21 91111
C20
C21
C22
C30
CR1
C18
C17
R32
19 74LS08
20 74LS132
C15
C16
R23
9 74LS109
11 74LS02
12 74LS04
13 8224
R21
C14
14 8080A
C10
C11
R19
15 74LS257
16 74LS257
17 74LS174
18 7425
C12
C13
R20
R22
D2
R18
C9
R17
1 74LS13
2 74148
R1
R2
D1
R3
R4
R5
R6
R7
R8
R9
R10
R11
R12
RH
3 8T97
4 8T97
5 8T97
6 8T97
7 8T97
8 8T97
9 7407
R14
R15
CPU
8 INCHES

figure A-3



PolyMorphic Systems
Video Terminal Interface
VIDEO REV1.2 FRONT
REV1.2A
100001
KBD
GND
VIDEO OUT
IC44 LM323K
IC1 74LS161
IC2 74LS161
IC3 74LS02
IC4 74LS74
IC5 74LS132
IC6 8131
IC7 74LS00
IC8 74LS352
IC9 8097
IC10 8097
IC11 8097
IC12 74LS138
IC13 74LS161
IC14 74LS20
IC15 74S93
IC16 74393
IC17 74LS157
IC18 74LS157
IC19 74LS157
IC20 74LS189
IC21 91L11
IC22 91L11
IC23 91L11
IC24 91L11
IC25 91L11
IC26 91L11
IC27 91L11
IC28 91L11
IC29 96LS24
IC30 74LS00
IC31 7407
IC32 74LS24
IC33 N8T74
IC34 74122
IC36 74LS157
IC37 MCM6571A
IC38 74150
IC39 74150
IC40 74273
IC41 DAS412
IC42 74LS132
IC43
SWITCH
A10 A11 A12 A13 A14 A15
JMP1 JMP2 JMP3 JMP4 JMP5 JMP6 JMP7 JMP8
Y1
Q1
D1 D2

4. Assemble Video Board

Install DIP sockets:

Orient the PC board so that the gold plated contact of the bus connector is facing you and the large foil area is at the upper right. This is the TOP of the board.

According to assembly diagram, check-off list, and designation on board, install sockets on top of the PC board.

Install IC sockets

Check	Location	Component
( )	IC 1,2	16 pin sockets
( )	IC 3, 4, 5	14 pin sockets
( )	IC 6	16 pin socket
( )	IC 7	14 pin socket
( )	IC 8, 9, 10, 11, 12,13	16 pin sockets
( )	IC 14, 15, 16	14 pin sockets
( )	IC 17, 18, 19, 20	16 pin sockets
( )	IC 21 through 28	18 pin sockets
( )	IC 30, 31, 32	14 pin sockets
( )	IC 33, 34, 35, 36	16 pin sockets
( )	IC 37, 38, 39	24 pin sockets
( )	IC 40	20 pin sockets
( )	IC 41	24 pin sockets
( )	IC 42	14 pin socket
( )	SWITCH	DIP Switch
( )	J 1	14 pin sidewipe socket (keyboard)

Install resistors

Check	Number	Description	Color
( )	R1	470 ohm	
( )	R2 - R10	2200 ohm	red-red-red
( )	R11	1000 ohm	brown-black-red
( )	R12	2200 ohm	red-red-red
( )	R13	1000 ohm	brown-black-red
( )	R14	customer provided option for keyboard (see page 28)	
( )	R15	2200 ohm	red-red-red
( )	R16	4700 ohm	yellow-violet-red
( )	R17	2200 ohm	brown-black-red
( )	R18	4700 ohm	yellow-violet-red
( )	R19	100 ohm	brown-black-brown
( )	R20	220 ohm	red-red-brown
( )	R21	220 ohm	red-red-brown
( )	R22	82 ohm	grey-red-black
( )	R23	2200 ohm	red-red-red
( )	R24, 25, 26	1000 ohm	brown-black-red

Install diodes: BEWARE OF POLARITY

Check	Number	Description
( )	D1	1N5225
( )	D2	vacant (customer provided keyboard regulator)

Install transistor Q-1 2N5449 flat side toward top of board

Step completed.( )

Install capacitors

Check	Number	Description
( )	C1,2	0.1$_u$F Ceramic Disc Cap
( )	C3	100 pF ceramic disc
( )	C4 through C23	0.1$_u$F ceramic disc

Check	Number	Description
( )	C24	10$_{u}$F 25V tantalum (note polarity)
( )	C25, 26	0.1$_{u}$F ceramic disc
( )	C27	10$_{u}$F tantalum
( )	C28 option, customer provided	0.1$_{u}$F ceramic disc (suggested)
( )	C29 option, customer provided	10$_{u}$F 25V tantalum (suggested)
( )	C30	0.1$_{u}$F ceramic disc
( )	C31	10$_{u}$F tantalum
( )	C32	0.1$_{u}$F ceramic disc
( )	C33	10$_{u}$F tantalum
( )	C34	39pf
( )	C35	22pf
( )	C36	.0047$_{u}$F ceramic disc
( )	C37	0.1$_{u}$F ceramic disc
( )	C38	10$_{u}$F tantalum - Note: positive toward bus connector
( )	C39,40,41	0.1$_{u}$F ceramic disc
( )	C42	10$_{u}$F tantalum
( )	C43,44,45,46	0.1$_{u}$F ceramic disc

Install potentiometers:

Install 10K ohm pots at R27 and R28. Screw adjustments must be toward outside of board to be of practical value. Step completed ( ).

Install Male output connector at Video out location.
Note that the unit closely matches the diagram printed on the Video board.
Step completed ( ).

Install voltage regulators

At IC 43 install 12V regulator 78L12 ( ) check.

At IC 44 install LM323 and heat sink assembly. Pleace the heat sink over the large foil area so that all four holes line up. Then place regulator over the heat sink. Secure with 6-32 hardware. Solder underside after securing heat sink. Check ( ).

4.a Smoke Test

At this point your VTI board is completed except for installation of IC's.

Before installing the IC's the board should be "smoke tested". Connect your VTI to appropriate power supply and observe carefully. Any unusual odor or sign of smoke indicates an error that must be remedied before you proceed.

4.b Install integrated circuits

Check			PINS	FUNCTION
( )	IC 1	74LS161	16	Binary counter
( )	IC 2	74LS161	16	Binary counter
( )	IC 3	74LS02	14	Quad 2-input NOR gate
( )	IC 4	74LS74	14	Dual D flip-flop
( )	IC 5	74LS132	14	Quad 2-input NAND gate
( )	IC 6	DM8131	16	6 input comparator
( )	IC 7	74LS00	14	Quad 2-input NAND gate
( )	IC 8	74LS153	16	Dual 4-input multiplexor
( )	IC 9	8097	16	Hex tri-state buffer
( )	IC10	8097	16	Hex tri-state buffer
( )	IC11	8097	16	Hex tri-state buffer
( )	IC12	74LS138	16	3 to 8 decoder
( )	IC13	74LS161	16	Binary counter
( )	IC14	74LS20	14	Dual 4-input NAND gate
( )	IC15	74393	14	Dual 4 bit binary counter
( )	IC16	74383	14	Dual 4 bit binary counter
( )	IC17	74LS157	16	Quad 2-input multiplexor
( )	IC18	74LS157	16	Quad 2-input multiplexor
( )	IC19	74LS157	16	Quad 2-input multiplexor
( )	IC20	74LS139	16	Dual 2 to 4 line decoder

Check			PINS	FUNCTION
( )	IC21	91L11	18	256X4 bit static memory
( )	IC22	91L11	18	256X4 bit static memory
( )	IC23	91L11 memory option	18	256X4 bit static memory
( )	IC24	91L11 memory option	18	256X4 bit static memory
( )	IC25	91L11 memory option	18	256X4 bit static memory
( )	IC26	91L11 memory option	18	256X4 bit static memory
( )	IC27	91L11	18	256X4 bit static memory
( )	IC28	91L11	18	256X4 bit static memory
( )	IC29	74S124	16	Dual gated voltage contrid osc.
( )	IC30	74LS00	14	Quad 2-input NAND gate
( )	IC31	7407	14	Hex open-collector buffer
( )	IC32	74LS74	14	Dual D flip-flop
( )	IC33	74LS157	16	Quad 2-input miltiplexor
( )	IC34	74123	16	monostable multivibrator
( )	IC35	N8274	16	Ten bit shift register
( )	IC36	74LS157	16	Quad 2-input miltiplexor
( )	IC37	MCM6571A	24	Character generator
( )	IC38	74150	24	16-input multiplexor
( )	IC39	74150	24	16-input multiplexor
( )	IC40	74273*	20	8 bit register
( )	IC41	74S412 or 8212	24	8 bit latch
( )	IC42	74LS132	14	Quad 2-input NAND gate

4. c Option Selection

Though the VTI is an integral part of the POLY 88 system, it is compatble with other systems. We have therefore, included a number of additional jumper option areas which do not apply to POLY 88 owners.

These are Jumper areas 1, 2, 3, 5 and 6.

*The polarity may be ambiguous; the oblong groove indicates the device orientation.

JMP1 changes the divide ratio from the system clock to produce scan rates which are more appropriate when using different system clock rates.

JMP2 selects the vectored interrupt priority for the keyboard input. The VTI is already wired for interrupt priority 2.

JMP3 and JMP6 are similar to JMP1 in that they adjust the scan rates when used with different clocks.

JMP5 allows use of an on-board clock.

4.d Select Character line length option.

Your board is configured for a 64 character line. If you require the 32 character line cut the trace on the back of the board between the middle pad of JMP4 and the pad designated 64 at JMP4. If you do not require the 32 character line, do nothing.

4.e Address location:

The VTI interacts through the S-100 bus as a block of memory and input port for keyboard. The memory block, (½ or 1 K bytes, depending on option) can be located at any address from Ø through 63 K in 1 K increments. (Software writter for this product will usually locate it at hexadecimal address F800).

Location is determined by comparing the six most significant bits of the memory address with six jumper selected bits. Reducing circuit complexity, the memory block also determines the address of the input port. The six most significant bits of the input port address must match the six switch or jumper selected bits. The two least significant bits are not compared for input address therefore, their state is arbitrary.

The address selection switch area is located at the lower left hand corner of the board near IC6.

Each of the six most significant bits of the address is resistor tied to + 5V, so that they are normally in binary state 1. Any or all of them may be grounded to cause a situation of binary state Ø. A DIP switch is provided for selectable jumpering. Typically, the address line on the right is grounded to the pads at left, producing a logical zero. The five switches nearest bus connector should be in the off position. The remaining two switches should be on, setting the board at F8ØØH.

4.3 Interface TV monitor or TV receiver:

At this point, your unit should operate if connected via coaxial cable to either video monitor or slightly modified receiver. (For the Hitachi line, an inexpensive TV receiver modification kit is available through PolyMorphic Systems).

If the prompt character does not appear on "power up", horizontal frequency adjustments, found on the back of the video unit, may be required.

Because of rigid FCC regulations, the circuit has been designed for direct connection to the video input circuit of the video amplifier, which is located between the last video IF stage and the video output circuit.

When the circuit is broken at video amplifier input, a DC bias circuit for the stage will probably be necessary, since in most cases it is supplied from the video IF amplifier. The optimum interface circuit will vary, but frequently a capacitive coupling to a resistive bias circuit is adequate.

The coupling capacitor is typically a 1-5$_u$F tantalum, oriented with the positive side connected to the video input amplifier.

IMPORTANT: Check to see that the chassis of your TV is isolated by a transformer from the 110 VAC line. If the chassis is not so isolated, but rather a polarized plug has been used on the line cord, FATAL INJURY COULD RESULT from possible electrical shock. If you must use this type of set, either isolate it with a transformer or isolate the video signal with an opto-isolator between the video terminal interface and the video input connection to the TV set. Under no circumstances should the polarized plug be trusted to maintain the isolation from the line voltage.

4.4 Connect keyboard

At the upper right hand corner of the video terminal interface board is the keyboard input port. This port provides a latched 8 bit parallel input capability which completely interfaces with many ASCII keyboards. Keyboards usually indicate a keystrike to the computer via a strobe line, in addition to the eight parallel input lines. The signal on this line changes state -- from high to low or from low to high -- to indicate a keystrike. Hookup varies according to whether the strobe on your keyboard is "positive going" (rising in voltage to indicate keystrike) or "negative going" (dropping to indicate keystrike).

4.4.1 Connector configuration

The parallel input from the keyboard is designed to come in over a ribbon cable terminated by a DIP MALE CONNECTOR. This plugs into the 14 pin DIP socket at the upper right hand corner of the board. The 8 parallel input lines are connected to pins 1 through 8 of this socket, (J-1) with 1 being the least significant bit. Pin 9 carries the "positive going" or "negative going," strobe. Pins 10, 11, and 12 are grounded.

Pin 13 is the output from the optional *negative voltage regulator. Pin 14 carries +5 volts as the primary supply for most keyboards. JMP8 allows 8 volts unregulated power at Pin 14 if desired. Be sure to cut the trace connecting 5 volts if you require this option. A jumper is inserted from the middle pad of JMP8 to the pad nearest the regulator within the area designated JMP8.

WARNING: FAILURE TO CUT THE TRACE SUPPLYING 5 VOLTS WHILE ATTEMPTING TO JUMPER IN 8 VOLTS WILL DESTROY EVERY COMPONENT ON THE BOARD AND VOID THE WARRANTY!

4.4.2 Keypress strobe

When the processor accesses the video terminal interface with an input instruction, the state of the keyboard input latch is transferred to the accumulator. Proper use of the keyboard requires that the processor must establish two conditions before using the input data. It must indicate that

1) a key has been pressed, and

2) this particular key depression has not been previously serviced.

These functions are accomplished by making the keypress strobe information available to the processor.

The keypress strobe line is an additional keyboard output line parallel with the data lines. This line signals each depression by a pulse. This test-function informs the processor that the necessary input conditions are met. The pulse:

1) interrupts the processor by setting an interrupt service latch contained on the input buffer,

* Used when the keyboard requires a negative supply. The user should select and obtain the components suited to his keyboard.

or 2) the interrupt request latch is available on data bit Ø of the status port; the keyboard strobe is available on data bit 7.

Attaching the strobe line of your keyboard to a VOM determine whether it is normally low (below .8V) or normally high (above 2.5V). If low, the jumper is already properly configured.

If high, cut the minus trace from center pad of JMP-7 and jumper from center pad to + labled pad.

i. <u>optional voltage regulator</u>

Provision has been made for the optional negative voltage regulator required by a number of keyboards. The pads and traces for this voltage supply are located adjacent to the keyboard input socket, just above the IC23. The supply regulates the -16V line by means of a resistor and zener diode stabilized by two capacitors. The four components are R14, C29, C28 and D2. The choice of resistor and zener values depends on the voltage and current requirements of the keyboard.

5. System checkout.

Install all boards and "smoke test" them. If something is obviously wrong, solve it before proceeding.

To test the POLY 88 system, you will want to hook it up to the video monitor.

In addition to a video monitor, you will need a simple logic probe with pulse detector. If you do not have one, buy one or build one using the circuit enclosed. If you cannot use a logic probe, do not attempt detailed checkout.

You will also need the VTVM or VOM you used earlier. A magnifying glass will also be helpful.

If the system does not operate properly, first eliminate the most common problems:

( ) 1. Check all components on all boards for proper location and orientation. In particular, check the tantalum capacitor orientation carefully.

( ) 2. Check all boards to make sure there are no solder bridges.

( ) 3. Check that all jumpers are in place, and that they are correct for either the 32 or 64 character option, whichever you ordered.

( ) 4. Check all boards to make sure tha all IC pins are correctly inserted -- not folded under or broken off, etc.

( ) 5. Check the jumpers or DIP switch on the video board for proper address selection.

If these problems are eliminated and the system still does not run properly, check the CPU board, using the logic probe pulse detector, to ensure that the clock signal from IC13 is available on pin 49 of the edge connector.*

If there is no clock signal, check for solder bridges and incorrect component placement and orientation on the CPU board. Check IC13 and IC8 (bus driver, 8197) using the list of chip pinouts at the end of this volume. Pins 10 and 11 of IC12 should have +2 to +8V. Use a VTVM for this test if your logic probe will not accept these levels. A malfunction at this point will usually produce a constant 0V or 10V. If you now have a clock pulse on pin 49 of IC13, and you still have system malfunctions, proceed to Video Board checkout, immediately below. If you still do not have a clock pulse, go directly to CPU Board checkout.

a. Video Board Checkout

If you have a clock signal, hook up the video monitor and power up. You should get a clear screen with the cursor in upper left hand corner.

The video board consists in essence of three areas: Sync, Data Bus, and Character Generation-Video.

If you have a coherent, stable, but useless display, the problem is most likely in Data Bus.

* Pin 49 is the second pin from the right on the top of the board (49th from left).

If you have no display, the problem is most likely in Character Generation-Video.

One problem that affects all three areas is the output buffer, so begin by checking pinouts on:

( ) IC 31 (output buffer, 7407).

Next, perform the relevant steps below.

Data Bus

( ) Check all RAMs, ICs 21 through 28 (91L11 or 2111).

( ) Check all RAM pins for proper insertion

( ) Check for solder bridges on RAMs and in the bus driver area.

Character Generation-Video

( ) Check the dot clock chip, IC 29(74S124).
If you have a display, you can check IC29 by decreasing the display width by adjusting potentiometer R27. If the display changes, the dot clock chip is probably defective.

( ) Check the shift register, IC 35 (8274).

If you have done all the above, and still have system malfunctions, continue with detailed checkout below. If a synchronized array of characters cannot be achieved by adjustments of sync controls on the CRT (or TV), check first for the more obvious and frequently encountered problems. Most typical will be such items as:

1. Loose connections to system or to display.
2. Improper interfacing to display's video input (biasing, etc.).
3. Omission or improper installation of components on the board (reversed diode or chip orientation).
4. Soldering problems of unsoldered contact or solder-bridge shorts.
5. Omitted or wrongly selected jumper patterns (line length, address selection, etc.).

The discussion below follows one of many possible logically sequenced procedures to localize problems and is written for those without access to an oscilloscope.

Start with a good visual inspectioh of connections and of the board itself. Progress through checks on the power supply busses and video output to electrical test patterns of the signals on the board. In using the electrical test patterns, work from end results backwards towards those parts of the circuit which contribute to the end results. For example: if the proper raster sync signals are doing their job, all further measurements concerning these circuits involved can be omitted in favor of checking contributions to character presentation.

a.1 Power mains

a.1.1. If visual inspection looks good, see if the power mains are proper. There should be +5.0 ± 0.2 VDC on the VCC bus. Convenient clip lead points include:

A. Ground reference: the metallized board area under the voltage regulator heat sink at the top right is a good one. The board has been designed with a blank area on the reverse side so that the other jaw of a clip cannot short any signals there. (Watch out for this at other locations, especially along the top of the board.)

B. 5 volt bus: the bottom lead of resistor R12. A voltage below tolerance here may indicate either a heavy current load from a misconnection or a reverse-oriented IC or that your power main feeding the board has less than 7 volts available.

Zero volts at this point probably indicates missing power to the board (a cold regulator) or a dead short on the board in which case the regulator will be very hot to touch. (Don't panic. You will be amazed at its recuperative capability when the short is cleared.)

C. VDD bus for the character generating ROM IC36(6571-4). Measure +12V± 10% at the junction of R20/C29.

D. VBB bus for IC37: Measure -3V ± 10% at the left hand lead of D1. (This is the only negative voltage.)

a.1.2 If power bus shorts are suspected, ohmmeter verification involves considerations of the polarity of the test leads. The board will not suffer from checks where the ohmmeter leads apply the polarity expected from the power supply and an open circuit voltage not exceeding the power supply value. The non-linearity of the load prevents us from predicting what an unknown ohmmeter will read on a normal board, but readings below an ohm mean that you should look for a short or an inverted IC. Reverse polarity from ohmmeter leads can be damaging unless the current is limited to low values. Most series-connected 50 micro-amp movement VOM's are safe when only the 1.5 volt battery is used on the scale selected.

a.2 Signal tracing

Unsolder the right end of the 100 ohm R1 (junction with pins 2, 4, 6, of IC31---- 7407) and attach a clip lead to the free end of the resistor for use as a scope probe. (Keeping a wire in the hole for the right end of R18 makes an easy way to remake the "normal" connection with the clip lead.)

DC voltages would normally read 1.6 V at this junction, but, when open, the clip lead will read about 4.5 and the IC31(7407) pins less than 0.1 V. This produces DC levels at the 2N5449 emitter of about 2V normally (average of normal waveform) and near 4V with an open test lead. 27% of these values should be found on the cable to the CRT. (If you have D.C. coupled into your CRT video, check that your design is proper for these values.)

Those users owning oscilloscopes probably have sufficient technical background to interpret the following discussion into equivalent scope presentations. This discussion assumes that the only signal tracing display available is the TV or CRT intended for computer display use. Therefore, the first checks are that the output stage is functioning and that its responses are visible on the CRT. If NOGO on these, check your cable and CRT. input arrangement.

a.2.1 video interface

Grounding the probe lead should pull the output emitter down to around a volt, and opening it should give a rise to around 4v. This transition should couple through the AC coupling to your CRT and be apparent as momentary brightening as the lead opens.

a.2.2 localizing on the video path

If logic levels applied to the clip lead are modulating the display brightness, but you are having to troubleshoot, let us consider what is missing. If, in the "normal" connection (i.e: lead clipped to where R19 should be soldered), there is an array of bright and dark spots on the display, chances are that video is being generated and that you will be chasing sync or blanking troubles. With only video coming through, most CRTs will at least partially sync on the video itself, and patient tinkering with the sync controls on the display and the two pots on the video board should give at least some torn-up version of what is trying to be a display. If you have sophisticated your power-up sequence to program a blank display, either alter the sequence until troubles are cured or remove programming to the board. Random states in the board RAM at power-up will produce some interpretable static pattern. But maintain the system clock connection. Horizontal sync is derived from that clock. (The board is testable with nothing more than proper power supplies and a clock for inputs.)

No video pattern? Let us see if it is shifting out of the register IC35-6(8274) (pin 6 of IC35). Got it? Then the path through IC31 is not passing it. Check for it at the input pin 9 and output pin 8 of IC31. Following the path should reveal a gap in signal passage that is correctable. This is the concept of signal tracing that will be assumed throughout the remaining discussion.

No video shifting out of IC35-6? Well, is there data on the input pins to be loaded for shifting - or a load signal to load it - or a dot clocking to shift it out?

First the dot clock on IC35-9(8274): This should show as a raster full of tiny white dots. Depending on the setting of the "width" pot, there should be from 100 or so to almost 900 on each raster sweep, but several factors influence this. Sync and blanking, if they are working, keep many dots out of the visible area. Also, the bankwidth of this setup may not permit you to discern dots at the higher frequency settings of the dot clock. Best to view this at the minimum frequency (ccw) setting of the "width" pot (pot at top left). Do not bother counting dots. Their presence is all that is necessary to show register shift clocking input. Since this signal is negative true, a brighter presentation may be found at the inverted form on IC30-8(74LS00). Absence of sync should not prevent this display from being recognizable.

EOC (end-of-character) loading signals on IC35-7 should show as dark (negative true) vertical bars every tenth dot (except for a portion of the screen where horizontal blanking normally disables the dot clock). Their presence proves the dot clock (and dot counter) whether we check IC35-9(8274) or not. The number of bars visible is variable by the dot clock frequency ("width" pot) and by the "pos" pot control of sweep blanking. Although the blanking path is broken by lifting R19, the composite sync path is not. Therefore, if a strong sync is at work, some of the display, such as the area unbroken by vertical bars, may be sync'd into times not visible on the screen. This point about sync must be borne in mind as you check many of the waveforms - particularly in the sync path itself.

Assuming that shift (dot) clocking and its subcount, EOC load clocking, are available, is there video data on the input pins to be loaded? Each of pins 1 through 5 and 11 through 14 should show a screen pattern of white and dark states as wide as the distance between the vertical bars seen on pins carrying the EOC or shift loading pulses. So too should input and output pins of the MUX's IC33 and IC36(74LS157). Also the outputs ROM IC37 (6571) and the graphics generators IC38 and IC39(74150).

The patterns associated with outputs from IC38 and IC39(74150) have a right to change every 5 sweeps. At the IC39(74273) inputs to the display generators IC37, 38, & 39, (6571) however, the sweep patterns should not change more frequently than every fifteenth sweep. These last patterns show what the memory is requesting for each character position of ten dots by fifteen sweeps. Counting these dimensions is generally not necessary. Merely noting that the fineness of detail is less at the input to generators than at the output is usually sufficient for trouble localizing. Subcounting is discussed under 3.2.3 and 3.2.5.

The screen pattern for any significant bit input to the generators should be traceable back through corresponding pins of the sampling latch IC40(74273) to the same significant bit of the internal data bus. But remember, the nth character in memory is held in the latch until an EOC pulse strobes the latch and increments the memory address. If sync and clocking are at work to keep the display pattern straightened up, any lack of correspondence of the patterns up the path can be discerned. Without sync, it may take both a photographic memory and a lot of luck -- but the chances are that you would not be needing that level of detailed trouble-shooting without sync, anyway.

In like fashion, grounding pin one of IC33(7LS157) forces MUX's IC33 and IC36(74157) to select only graphic symbols from IC38 and IC39(74150). This change is most apparent with a sync'd display, but some shift should usually be discernible in the pattern for any shift register input pin. The degree of change will depend on how frequently the MSB is a one in the RAM. Correspondingly, the display probe on IC33-1(74157) will show which memory locations contain graphics or non-graphics characters. An MSB in memory is inverted in the latch to select graphics.

a.2.3 localizing on the EOC (end of character) path

If you had dot clock input to shift register IC35-9(8274) but no stobe (IC35-7) to load the register, you will want to check back to where the EOC is generated by counting every tenth dot in IC14. In fact, failure of IC30(74LS00) or other problems can permit it to count by other than ten, with some weird results in displays. Clock dots are discernible at the input IC13-2. Slowing the dot clock (CCW on the "width" pot) makes these countable by eye. A piece of paper on the screen or a millimeter scale may help. Sync helps here but should not be necessary to array the pattern of dots into vertical bars. IC13-14(74161) has half as many vertical bars but of double width. Pin 13 has narrow vertical white bars equal to twice the width of the bars on pin 14. The total pattern of pin 13 is repetitions of black, white, black, white, white vertical bars. The last two whites show as a double width white as the carry preloads a 6 into this 4 bit binary counter. This preload makes it produce a carry every tenth dot. If pin 13 looks right, chances are that all the rest is okay.

The tenth dot carry on IC13-15 is the EOC (end of character) signal. It should appear at the input to the symbol counter IC16-13. An inverse (negative true) of this pattern should be found as loading signals n latch IC40-11(74273) and shift register IC35-9. Of course, if there is no dot clock, none of this paragraph is working properly. On the other hand, presence of dots anywhere does not leave much room for problems in the dot clock.

a.2.4 localizing on the dot clock path

If either the shift register or the dot counter is getting dots, you are in for some detail checks of solder bridges to ground, a single NAND gate in IC30(74LS00), or some such, because the clock is present at the other end of these places. If neither is present (and of course no EOC signals), then look for dots at the clock IC29-7(745124). Using a voltmeter, check its "width" pot for the ability to vary IC29-2 from zero to 5 volts. Check also for the enabling portion of the horizontal blanking signal on IC29-6. This may be hard to see as a broad vertical bar in the presence of strong horizontal sync, but if desyncing gives you a torn version of it, it is probably okay. A voltmeter reading on IC29-6 of 5 VDC would be a continuous disable signal. Under proper conditions, the average of the horizontal blanking waveform reads typically 0.9 to 2.3 VDC on a meter at IC29-6. The value is under control of the "pos" pot which varies the time delay (and thus the average DC value) of the blanking monostable.

a.2.5 <u>localizing on the horizontal blanking path</u>

Under the most ideal conditions of sync and blanking, events occurring during flyback, retrace, or blanking should not be visible. Note that opening R19 does not open the composite sync path at IC31-10(7407). Therefore, sync, if operating, will reach the CRT sync circuits - regardless of what is done with the probe lead. Remember, even without sync working, most CRT's or TV;s will find in many of the test signals something repetitious enough to sync on. There is usually a way to view sync-hidden signals by misadjusting the horizontal hold control of the CRT to force a "tear" in the picture. Then if the sweep rate is calibrated in time units, the signal can be measured in the torn portion. An example of this is horizontal blanking. Forcing a torn but stable pattern reveals a dark space in each sweep when looking at IC29-6 (74S124). Varying the "pos" pot changes the width of the space.

Typical values from stop to stop on the pot are about 10 or 20 microseconds (see section 3.3.1 on time calibration) but, if you can change it, it is working. Perhaps easier to see is its inverse - a logic high on IC34-5(74123). For this, you should not have to force the tear. Horizontal blanking that is high logic will appear as a bright vertical bar at one or both sides depending on where the CRT is syncing. For most IC's, if Q is working, $\overline{Q}$ probably is also. Take the easiest way down the localizing path first and back up to the harder ones only when necessary.

No horizontal blanking? How about the horizontal sync which triggers the IC34 monostable multi-vibrator to stretch the sync into a wider blanking? The carry out of counter IC1-15(74161). should have its inverse on IC34-9(74123). This is a 4½ micro-second pulse every 58½ microseconds.

Actual horizontal sync is the same width, but 4½ microseconds later, and can be seen on IC3-13(74LS02). Its inverse is on IC3-1 but is also mixed with vertical sync. Observation of a once-per-sweep, narrow vertical bar is probably sufficient to eliminate further details up this path, but if things are not clearing up, you may want to calibrate time as in a.3.1.

If these are NOGO, is the system clock on edge pin 49 and is it reaching IC2-1(74161)?

You can use your piece of paper or plastic millimeter scale to ratio the distance between leading edges of the bars. However, if the vertical bar pattern on IC2-14 is repetitions of black, white, black, white, black, white, black, white, white, then the binary 7 is apparently preloading on every carry and division is probably okay. (Compare this with the discussion of the dot counter in a.2.3.)

Counting bars will only tell you how many of the 58½ microseconds per sweep are visible on your CRT and usually does not contribute to trouble analysis.

IC2-2 has an inverted form of IC1-15 showing a dark bar every 4½ microseconds, but division by 13 is difficult to ratio unless you have a rare CRT that has a horizontal width control that permits shrinking the picture sufficiently to see both ends of the sweep. But then - if any of IC2-11(74LS138), IC2-13(74161), IC2-15, or IC3-13(74LS138) have an observable once-per-sweep bar, horizontal sync seems to be doing its job.

a.2.6 <u>sweep and symbol related counter patterns</u>:

Verification of <u>sweep counter</u> test patterns is difficult in the absence of horizontal sync. Since the sweep counter is counting the carries from the same counter that generates horizontal sync, the presence of one signal without the other would indicate that the integrity of any missing path should be reestablished before proceeding. The clocking input IC15-1 (74393) is a once-per-sweep pulse which may not be in the visible portion of the sweep unless a tear is forced in the horizontal hold. All other patterns are stretched by the sweep into horizontal bar patterns with the exception of the reset IC15-2. The reset is like the clock on IC15-1 except a) it occurs every 15th sweep; b) it is a 4½ microsecond darkening instead of a brightening; and c) it occurs 4½ microseconds later (to the right) on the screen. It is therefore probably visible only under torn conditions.

Correct patterns for pins 3, 4, 5, and 6 of IC15 can be inferred from the timing diagrams. A quick check of proper operations and counting by fifteen can be made on pin 4. The pattern for IC16-3 is: every other pair of sweeps is white (2nd, 4th, and 6th pairs) followed by the single white 15th sweep during which the counter is reset. Symbol lines are perhaps better defined by the double black sweeps visible on IC15-13. These occur because of the adjacency of the first and last sweeps, which are both dark, while all even numbered sweeps including those during retrace are bright.

As further subcounting is done in the line counter, IC15-11 shows every other line (group of 15 sweeps) as dark or bright. Forcing a tear in the horizontal sync can permit staggering the gap caused in each sweep. This can permit an alternate form of checking division by 15 (sweeps per line) in the sweep counter.

The MSB in the line count is white in the bottom half of the display. After the bottom bright trace of IC15-8, IC2-9 shows the bright inverse of 8 sweeps of vertical blanking at the bottom of the screen and the later sweeps normally hidden by the vertical blanking at the top of the screen.

Patterns for the symbol counter IC16(74394) can be directly inferred from the theory discussion and the pin outs of the 74393. The EOC pulses described in a.2.3 are seen as a vertical bar per symbol space on IC16-13. Successive divisions by 2 on pins 11, 10, 9, 8, 3, 4, and (if 64 symbol option, pin 5) are seen as fewer, wider bars. Reset will appear on pins 12 and 2 as it does at IC34-5 (Refer to Section a.2.5.)

The functions of IC12(74138) and IC34(74123) are not directly observable in the presence of sync. If no sync at all is reaching the raster, normal operation of IC34-13 can be noted as small (on the order of 30 nanoseconds)specks scattered in regular fashion throughout the raster. If sync is working, operation may be inferred by noting rapid regular jumping of vertical sync when IC34-1 is held to ground.

The combination of IC34b and IC12 can be checked by grounding pins 4 and 5 of IC3. Under this condition, the normal output connection to the display will show repetitions of seven darkened sweeps of vertical blank followed by thirty visible sweeps of retrace allowance. Also, placement of the test clip on IC12-12 will show continuous repetitions of seven dark sweeps, eight white sweeps, seven dark, fifteen white.

The outputs of the symbol and line counters should show obvious ÷ 2 relationships for ascending orders of bits. These patterns should be traceable through the MUX's IC's 17, 18, and 19(74157) and decoder IC11 to the associated RAM address input pins.

Normal events on the dot blank flip-flops IC32-2, 4, 5, and 8 (74LS74) produce vertical bars on a once per sweep basis. Position and width of the bars is variable by both "pos" and "width" pots. The waveform average of these waveforms read on a DC meter will also vary under control of these pots. If sync prevents visual observation of these pulses, DC voltage variations by the pots can be taken as proof that the variable width dot blank is reaching the right places.

a.3 Diagnostic aids

Viewing the display in normal conditions gives information on where to start troubleshooting. A blank screen directs attention to sections 3.2.1 through 3.2.5, which look for dynamically changing patterns originating in a sequentially scanned memory, being translated in the ROM's and being shifted out of the register. In the process, dot clocking and EOC signals are investigated as necessary.

A dynamic but useless display in normal conditions, on the other hand, directs attention to the subcounters and decoders which control memory address, the blanking of the display borders, and the orderliness of symbol element display.

Thoughtfully examining the display can give valuable clues for trouble locallizing. Torn-up symbols logically relate to the sweep counter and its derivatives in the line counter and vertical blanking. Wrong symbol displays indicate a need to also verify dynamic signal paths between symbol and line counters, or the ability to load memory properly. Since many of these are interrelated in unpredictable syndromes, it is impractical to anticipate all combinations here. Problems relating to data exchanges between the memory and/or keyboard and the system CPU are not peculiar to the video display and should be approached in whatever is your standard method for handling problems with memory or peripherals.

a.3.1 time calibration

In verifying the timing diagrams related to horizontal sweep rates, the 4½ microsecond wide bars on IC1-14(74161) give a quick idea of how much of the timing diagram will show on your TV. A 50 microsecond block is indicated on most of the timing diagrams, but a typical TV might show five white and give black bars on IC1-14 for a total display of 45 microseconds. Remember also that horizontal sync may permissibly vary widely, so that your picture may start at a different point in comparison to the arbitrary marks on the diagrams.

Calibration of the vertical dimension or vertical sweep time base is perhaps easiest by looking at IC15-3(74393). The leading edges (measuring top to bottom) of the groups of white sweeps are 15 sweeps or 877 microseconds apart. A 16 line (240 sweep) visible raster is 14.04 milliseconds, and vertical sync recurs every 277 sweeps or 16.205 milliseconds.

Occasionally, an integrated circuit is itself defective. You can sometimes determine this by swapping ICs from one location on the board to another -- i.e., ICs that are used in more than one location (like memory). If you find that you were supplied with a defective chip, it will be replaced free (see the warranty information sheet included herein).

b. Central Processor Checkout

A malfunctioning central processor may not produce enough behavior to allow testing. For that reason, the following checkout procedure is limited. Checkout beyond the limits of this discussion should be performed by someone with a thorough knowledge of data processing electronics.

Begin by checking the data bus, pins 3 through 10 on IC14 (CPU), and the address bus, pins 25 through 27 and 29 through 40, for shorts to each other, to the power supply, or to ground.

Put your logic probe on pin 12 of the CPU chip. Logic should be low. Push RESET; logic should go high while RESET is held down. If the logic is otherwise, check IC13, the RESET button wiring, and the 33 µF capacitor. Check also for cold solder joints along the path from pin 75 of the bus to pin 2 of IC13.

Signal is high when RESET is held down, check ICs 17 and 30 (74LS174) and IC38 (74LS109) to see that the POC-signal is low. It should go high when RESET is released.

When you push RESET, the screen should clear and a prompt character appear in the upper left corner. If this does not happen, the CPU chip is not running. Check for a "reading" signal on pin 23 of the CPU chip. The signal should be high. If it is not, check ICs 13, 40(74LSØØ) and 1 (74LS13).

Now check for a sync signal on pin 19 on the CPU chip. There should be a pulse. If there isn't, hold down RESET and check to see if the signal is low on this pin; releasing RESET should cause momentary or continuous pulsing. If you are not getting the desired sync signal, check the board again for solder bridges with a magnifying glass. If the sync signal cannot be obtained, further checkout will require a high-quality oscilloscope and considerable experience.

If you do have a sync signal, check pin 9 of IC17(74LS174) for pulses. If the sync signal isn't getting through to that point, check ICs 17, 13, 41(74LS109), and 12 (74LS04). If there is a pulse on pin 9 of IC17, but the system still does not work, further checkout will require a high-quality oscilloscope and considerable electronics experience. At this point, if you are not able to continue checkout on your own, you should talk to a knowledgeable friend or fellow club member, to the personnel at the store where you bought your system, or to the manufacturer.

B: Theory of Operation

1. Video Terminal Interface

a. Block diagram

The principal functional blocks which form the video terminal interface are shown in figure B-1. The on-board memory is connected in parallel with the keyboard input port to an array of I/O buffers driving the Altair data bus. This allows the transfer of information between the memory and the data bus or between the keyboard and the data bus. These data transfers are controlled by logic driven from the address and control lines. For example, the processor can read or write a location in memory just as it would with any main memory--it outputs the memory address (16 bits) while signaling a read or a write by the state of the control bus. The six most significant address bits are compared to the jumper selected bits (as discussed in section 22). If these bits match, then the remaining 10 address bits are gated through to select the memory location. At this time the appropriate bus drivers are enabled to read from or write into memory, according to the control bus command. If the control bus signals neither a memory read nor a memory write, but rather an input instruction, then the keyboard buffer is enabled instead of the memory. Note that the input port address (8 bits) is the same as the most significant byte of the 16 bit memory address. When the processor is not accessing the video terminal.interface with an input or memory instruction, then the video refresh circuitry takes control of the memory. The memory locations are scanned by the control and sync generator, with the memory data being fed into a character ROM. This read-only memory stores the video dot pattern of each ASCII character. The character font is a 7 X 9 matrix, so that each ASCII character has 9 memory blocks 7 bits wide in the ROM. Thus each line of characters on the TV screen results from many sequential scans through a line of memory locations. Each scan increments a counter so that the

ROM reads off the next line of the dot matrix. Each clock of 7 bits read from the character ROM is loaded in parallel into a shift register and shifted out serially. This signal is then mixed with the video sync signals to form the composite video output.

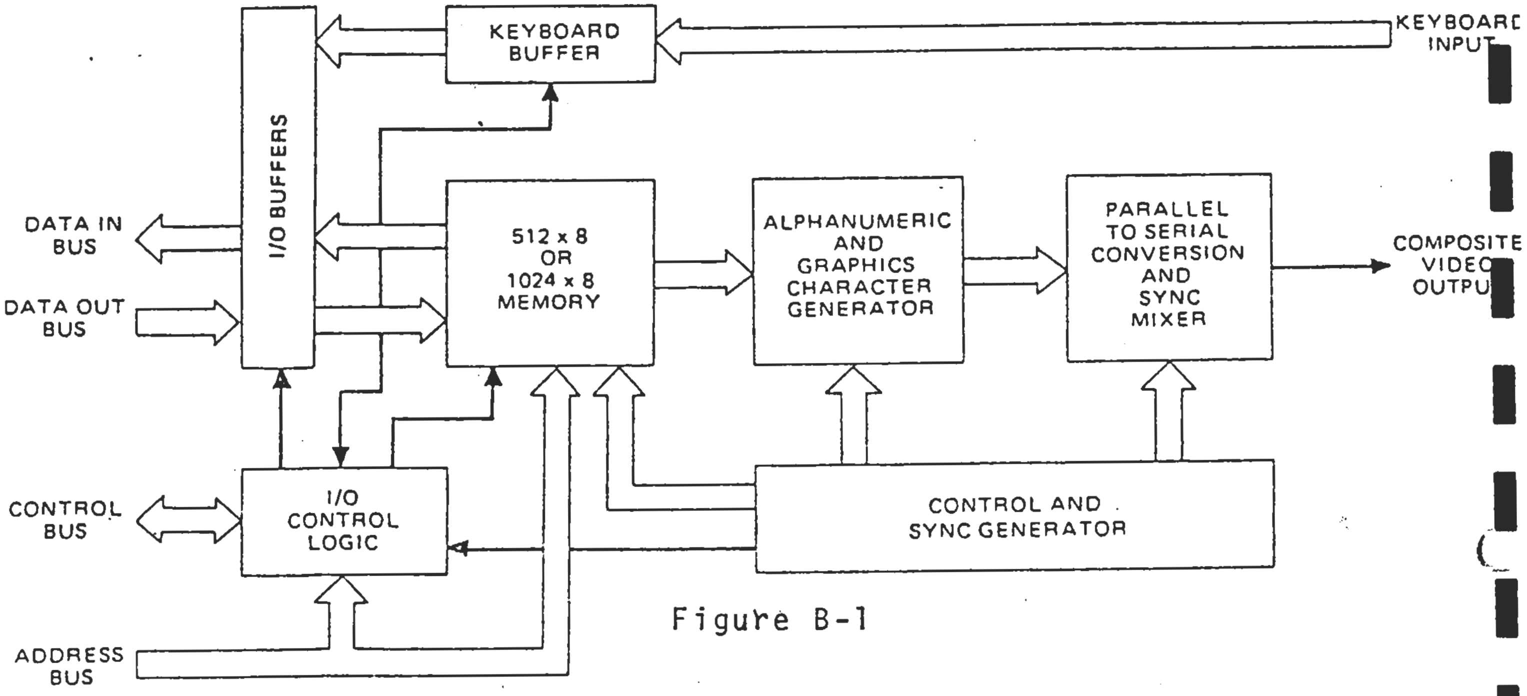

KEYBOARD BUFFER
KEYBOARD INPUT
I/O BUFFERS
DATA IN BUS
DATA OUT BUS
512 x 8 OR 1024 x 8 MEMORY
ALPHANUMERIC AND GRAPHICS CHARACTER GENERATOR
PARALLEL TO SERIAL CONVERSION AND SYNC MIXER
COMPOSITE VIDEO OUTPUT
CONTROL BUS
I/O CONTROL LOGIC
CONTROL AND SYNC GENERATOR
ADDRESS BUS

Figure B-1

b. Schematic diagram

A more detailed view of the board circuitry is shown in the schematic diagram at the end of this volume. We are now going to examine the board in some detail to see how it performs its various functions. The level of complexity is fairly high; not all readers will find it useful.

Look at the schematic and note that all the on-board memory, data latches, and bus drivers are connected to a common on-board data bus. This bus can be driven by, or can drive, the Altair's own data bus. We will be referring to the video terminal interface (VTI) data bus as the on-board bus, and the Altair bus as the external bus.

Another point of terminology is sweep vs line. Each character on the TV screen consists of a selection of dots in a dot matrix that is seven dots wide by nine high, embedded in a field of ten by fifteen dots (to provide space between characters). So the TV picture tube must sweep fifteen times to produce one line of characters.

The following discussion applies equally to the 32-character line and the 64-character line options.

b.1 symbol generation

With a low on the OE (output enable) line from IC9 to the RAM (random access memory) pins 9, the addressed portion of the RAM is continuously sent to the internal data bus in the refresh mode. Eight-bit display data on the internal data bus is sampled and held in the latch IC40 whenever there is coincidence (in IC30) of a dot pulse from the dot clock IC29 and an "end of character" (EOC) signal (tenth dot carry) from the "dot counter" IC13. In the absence of a one in the MSB (most significant bit) from the latch, MUX's (multiplexors) IC33 and IC36 pass the seven-dot conversion pattern of this display data from the character-generating ROM (read-only memory) IC37 to the 7 LSB (least significant bits) of the output shift register IC35. When the eighth bit specifies that graphics are being genrated, these MUX's switch to select all ten bits of the data for the shift register from IC38 and IC39. IC37 and IC38 are, in effect, the graphics genration ROM.

In the case of non-graphics characters, the first three dots of every character space are always low to create spaces between letters. Note that, while the latched data for the nth character position of the sweep is identical for fifteen consecutive sweeps, the ROM output may vary in each sweep, according to the additional addressing from the sweep counter half of IC15. The sweep counter is self-resetting after every fifteenth sweep, and this resetting action is accumulated in the line counter half of IC15.

In similar fashion, the dot counter IC13 is self-resetting every tenth dot, and its output is accumulated in the symbol counter IC16. The combination of line and symbol counter outputs determine the address of each individual character stored in the memory (IC's 20 through 28). Since all of these counters (dot and character, sweep, and line) are reset by appropriate relationships to the horizontal and vertical sync (respectively) of the TV raster, the lowest memory address will always contain the record for the top left corner of the TV display. Corresponding relationships are similarly maintained between other addresses in memory and positions in the display field.

b.2 raster & timing

Horizontal sync, vertical sync, and vertical blanking are timed by subcounting the absolute frequency system clock. Horizontal blanking is initiated at the end of sweep by subcounting the variable frequency dot clock IC29, and blanking is maintained by a variable-duration one-shot IC34. Varying the "pos" pot changes the one-shot delay and thus the position in the next sweep where the display is again unblanked. Varying the dot clock frequency ("width" pot) changes the rapidity with which the full line character count will accumulate to initiate horizontal blanking and therefore the distance across the screen that is used for display.

The system clock is divided by nine in IC1 and again by thirteen or fourteen in IC2. A carry on exit from the highest (16th) state (all four output bits = 1, or binary 15) is used to preload a binary 3 into the same IC2 so that it may again divide by 13 or 14. This binary 3 at the IC2 outputs will therefore last for one-thirteenth or fourteenth of the period between carries and is passed through IC3a to the TV for horizontal sync. The same carry triggers the horizontal blanking one-shot. The carry is also used to clock the 4-bit binary sweep counter (IC15a) which is used both to address the character generation ROM and to signal the line counter IC15b every fifteen sweeps that a new display line is being addressed.

When 16 line counts (16 X 15 = 240 sweeps) have accumulated in IC15b, the carry resulting from the transition from its binary 15 state to its binary zero state is inverted by to set the vertical blanking flip-flop IC4. In addition to blanking the screen, IC4 also enables the 1 of 8 decoder IC12. After eight blanked sweeps have been counted by the sweep counter IC15, Pin 14 of IC12 will go low, producing a vertical sync pulse.

This vertical sync lasts the seven more lines until IC15a resets itself and advances the line counter. IC3 ANDs this vertical sync with the horizontal sync carry, so that the interruptions in the wide vertical sync pulse maintain horizontal sync.

Further subcounts of the sweep and advances of the line counter accumulate in IC15 until IC12 decodes the 37th blanked sweep to trigger the pulse stretcher IC34. (Line counter = 2 and sweep counter = 7.) IC34 is a very short duration one-shot which terminates the vertical blanking (disabling IC12) and also resets the sweep and line counters for top of the page addressing. The subsequent termination of horizontal blanking has the character counter IC16 reset to prepare all addressing from the top left of page as described below.

b.3 symbol and raster synchronization

Termination of the horizontal blanking one-shot IC34a reenables the dot clock oscillator IC29a but does not unblank the screen. At this time, symbol count addresses are set to zero, but the data latch IC40 contains unrelated data sampled with some previous address. Similarly, the shift register IC35 contains old data. The screen has been darkened by the dot blank flip-flops of **IC32** which have been held set by the horizontal blanking. The symbol counter IC16 MSB is presenting a zero to the D input of flip-flop IC32, however. After the first ten dots from the dot clock, the shift register (which is shift-clocked by dots) is emptied and the EOC (end-of-character) signal from the dot counter sends load signals gated through IC30 to both the data latch and the shift register. Since propagation time through the ROM's and MUX's is not zero, the latch now contains beginning-of-line data, but the register is loaded with different but still useless data. The same end-of-character pulses, however, have advanced the symbol address in IC16 by 1 and have also propagated the zero at the input of the first D Blk (dot blank) flip-flop to the second flip-flop. The ROM and MUX paths present valid first symbol data to the shift register so that the second EOC pulse loads first symbol dots into the shift register and second symbol data into the latch. They also propagate the zero through the second dot blank flip-flop so that the screen is unblanked for the first symbol data shifted out of the register by the subsequent ten dots.

When the 32nd (or 64th) end-of-character pulse accumulated in the character counter, it loads the data latch with the 32nd (or 64th) character and the register with the next-to-last character. Simultaneously, the MSB of the symbol counter presents a 1 to the dot blank flip-flops, and the next 20 dots shift the last two symbols out to the video, and the 1 through the flip-flops to blank the screen in the 33rd (or 65th) character position. The dot clock runs, and the dot and symbol counters keep accumulating, but the MSB of the character counter maintains its 1 input to the dot blank flip-flops until either double the number of symbols is counted or, as normally, horizontal sync and horizontal blanking occur to stop the dot clock, reset the symbol counter, and reaffirm the dot blank.

Clocked by the sweep counter reset, the line counter will increment every fifteen sweeps until the vertical blanking process described above resets the MSB's of the addressing system.

b.4 external bus and keyboard interfacing

The comparator IC6 compares the 6 MSB's of the external address bus with the jumper pattern selected for display memory addressing. If these agree at the time IC5_ finds coincidence between system sync (pin 76) and Ø1 of the system clock (pin 25)

In the switched condition, RAM address is determined by the ten LSB's on the external address bus instead of by the combination of line and symbol counters used in the display refresh mode. The BS- strobe also enables the line drivers that put internal data bus information onto the external data bus. If INP+ (pin 46) is also true, keyboard data latched in IC41 will be sent to the CPU via the line drivers. The MEMR+ signal, if present, similarly enables the memory output to the on-board bus. If MWR+ (pin 68) is high with BS-, the line receivers are enabled by IC7s to transfer the external data bus to the internal data bus and write it into the onboard RAM. In this way, CPU data can be written into display addresses, keyboard data can be input to the CPU, or memory can be read from the display RAM addresses into the CPU. Keyboard data can be latched into IC41 in response to "key pressed" strobes of jumper selected polarity. Jumper provisions are made to copy this strobe on bit 8 of the keyboard input. A jumper pattern to pin 4 of the external bus permits sending an interrupt request to the CPU when the latch IC41 is updated by a "key pressed" strobe.

2. Central Processing Unit

a. Block diagram

The block diagram of the CPU board is shown in figure B-2. The functioning of this board takes place under the direction of the 8080A central processor. The processor can address memory or I/O ports via the address buss, and transmit or receive data via the data buss. Several additional control lines (not shown) allow the processor to indicate to the device addressed whether a memory read or write, or an input or output instruction is being performed. In general, programs are executed from ROM or RAM and intermediate results are stored in RAM, while serial communication is accomplished by input and output instructions to onboard I/O ports connected to the USART (Universal Synchronous/ Asynchronous Receiver Transmitters). Other onboard ports control the serial transmission speed (baud rate), single step, and off-board memory addressing. The priority encoder responds to externally generated interrupts to cause the 8080 to execute one of eight restarts as the next instruction.

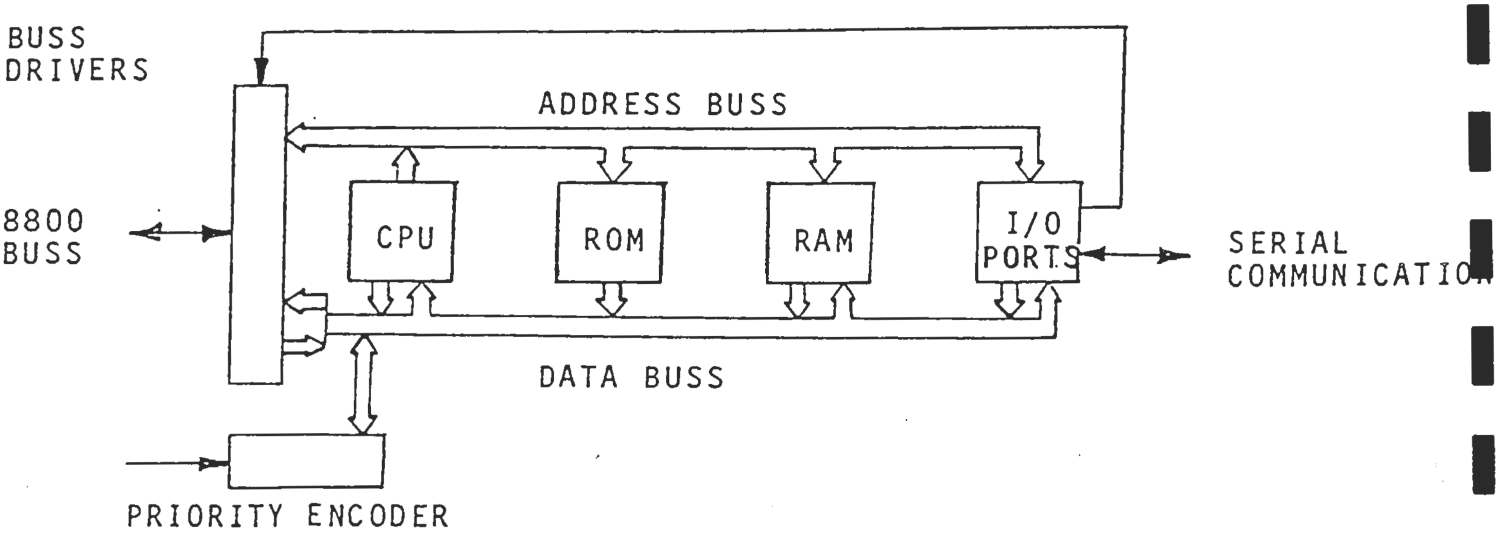


figure B-2

b. Schematic Diagram

The schematic in the appendix gives a more detailed view of the central processor board circuitry. To get full use of the following discussion of the schematic, it is necessary to have some familiarity with the Intel 8080A CPU chip. We recommend reading the Intel Microprocessor User's Manual, chapter 1.

Power Supply

There are four voltages on the board: +12, -12, +5, and -5. The power supply section consists of ICs 32, 33, 34, and 44, and the associated capacitors.

CPU

Clock signal generation is provided by IC 13, running at 16.588 MHZ. That oscillation is divided by nine and used to form a two-phase clock, ø (Greek phi) 1 and ø 2 on the schematic. (The 8080 requires two phases.) These clocks time all processing.

Ready and reset signals are synchronized to the clocks in IC 13. The ready signal to IC 13 is generated by ICs 1 and 40.

If (BGNT+ and XRDY+ and PRDY+) or ONBD- are active, then a ready signal is generated.

A reset signal is produced when pin 75 of the backplane goes low. On application of power, this line is held low momentarily by the 33 F capacitor and the 4.7K resistor.

The reset signal labeled POC (power on clear) on the schematic, generated by IC 13, resets the CPU, IC 14, status latch IC 12, and baud rate port IC 30. It also resets a part of the single step log, IC 38, and the USART, IC 28. This signal also goes out to the backplane for use by other boards.

During the T1 cycle (see Intel manual), the system strobe signal SSTB is generated by IC 13. This signal is used by the status latch to latch the CPU status for the duration of the memory cycle that follows.

The output of the status latch is used directly on the CPU board; it is also buffered by ICs 7 and 8 and goes on to the backplane. Both phases of the clock signal are also buffered in ICs 7 and 8 and sent to the backplane.

Clock phase ø1 is converted to TTL levels by the diode and the 2.2K resistor.

SYNC, DBIN (data bus in), and WR (write) strobes are buffered in IC 3 and also connect to the bus.

Data Paths

The CPU data bus is connected to the on-board ROMs amd RAMs, ICs 21 through 27, the USART, IC 28, and the baud rate generator port, IC 30. The data bus is also connected to ICs 5, 6, and 7, which are buffers leading to the data out bus on the backplane.

Data in from the backplane comes through ICs 15 and 16, two input multiplexors. Other multiplexor input comes from IC 2, the priority encoder. This IC encodes eight interrupts into eight restart instructions, RST Ø through RST 7.

Address Decoding

The CPU address bus is connected to ICs 21 through 27 (RAMs and ROMs), and to the address bus on the backplane through ICs 3 through 6, tri-state buffers. The lower eight bits of the address bus are connected to RAMs ICs 21 through 24. The upper four address bits are connected to IC 35, which generates signal ONBD- when all four bits are low. This determines whether on-board or off-board memory is accessed. If off-board memory is being accessed, ONBD is not active. If it is not active, there is no ready signal to the CPU till BGNT and XRDY and PRDY are active. If they are not active, the CPU waits till it can get access to the bus and till the device it is addressing is ready. Access to the bus is determined by BGNT (bus grant); XRDY and PRDY indicate that the addressed device is ready.

For accessing on-board memory, address decoder IC 36 is enabled via a connection to the EØ input (enable Ø) except when in an interrupt acknowledge cycle, in which case E1, connected to INTA+ (interrupt acknowledge), will be high, which inhibits IC 36.

Decoder IC 36 decodes the next two lower address lines, A1Ø and A11, along with the signal indicating whether we are in a memory cycle or an input-output cycle. The I/O select signal is generated by IC 37, which ORs together input and output status signals from the status latch.

The decoder generates eight output signals. Three of them select one of three on-board ROMs; these signals are ANDed with DBIN in IC 39 and applied to chip selects on ICs 25, 26, and 27. These three signals, MSØ, MS1, and MS2 correspond to address Ø through BFF hex. The fourth memory select signal, MS3, enables on-board RAMs, ICs 21 through 24, for addresses cØØ through FFF hex.

Further address decoding is provided by IC2, which is connected to A8. The remaining four signals, PSØ through PS3, select on-board I/O ports. PS Ø selects IC 28, the USART. Address decoding also is provided by AØ, connected to pin 12 of IC 28. The USART is located at addresses Ø through 3. Addresses 4 through 7, PS1, select the baud rate port, IC 30. Addresses 8 through B hex select the real-time clock, which uses ICs 20, 10, and 37. PS3, at addresses C through F hex, selects the single-step logic, which uses ICs 37, 38, 40, and 41.

Serial I/O Port

Circuitry for the optional serial input-output port consists of the USART IC 28, baud rate generator IC 29, baud rate port IC 30, buffer IC 31, and NOR gate IC 18. The clock signal for the USART is generated from ø2 of the system clock by division by two in IC 38 and further division in IC 29; the division ratio is selected by the data held in output port IC 30. The resulting frequency goes to the USART and through the buffer in IC 31 out to the serial I/O device, which connects to one of the 14-pin sockets on the CPU board.

The USART converts serial data to parallel form and puts it on the data bus for the CPU, or takes parallel data from the CPU and converts in to serial form.

The NOR gate, IC 18, ties the USART to the vectored interrupt system.

Real-Time Clock

The real-time clock is derived from a 60HZ rectified sine wave present on the backplane. The sine wave is converted to a square wave in the Schmiddt trigger, IC 20, and toggles the flip-flop IC 10 on each positive-going transition. Output of IC 10 jumper pad A may be tied to the vectored interrupt system. IC 10 may be reset by writing to output port 8. This generates PS2- and WR-, which are ANDed together in IC 37 and used to reset the flip-flop.

Single-Step Logic

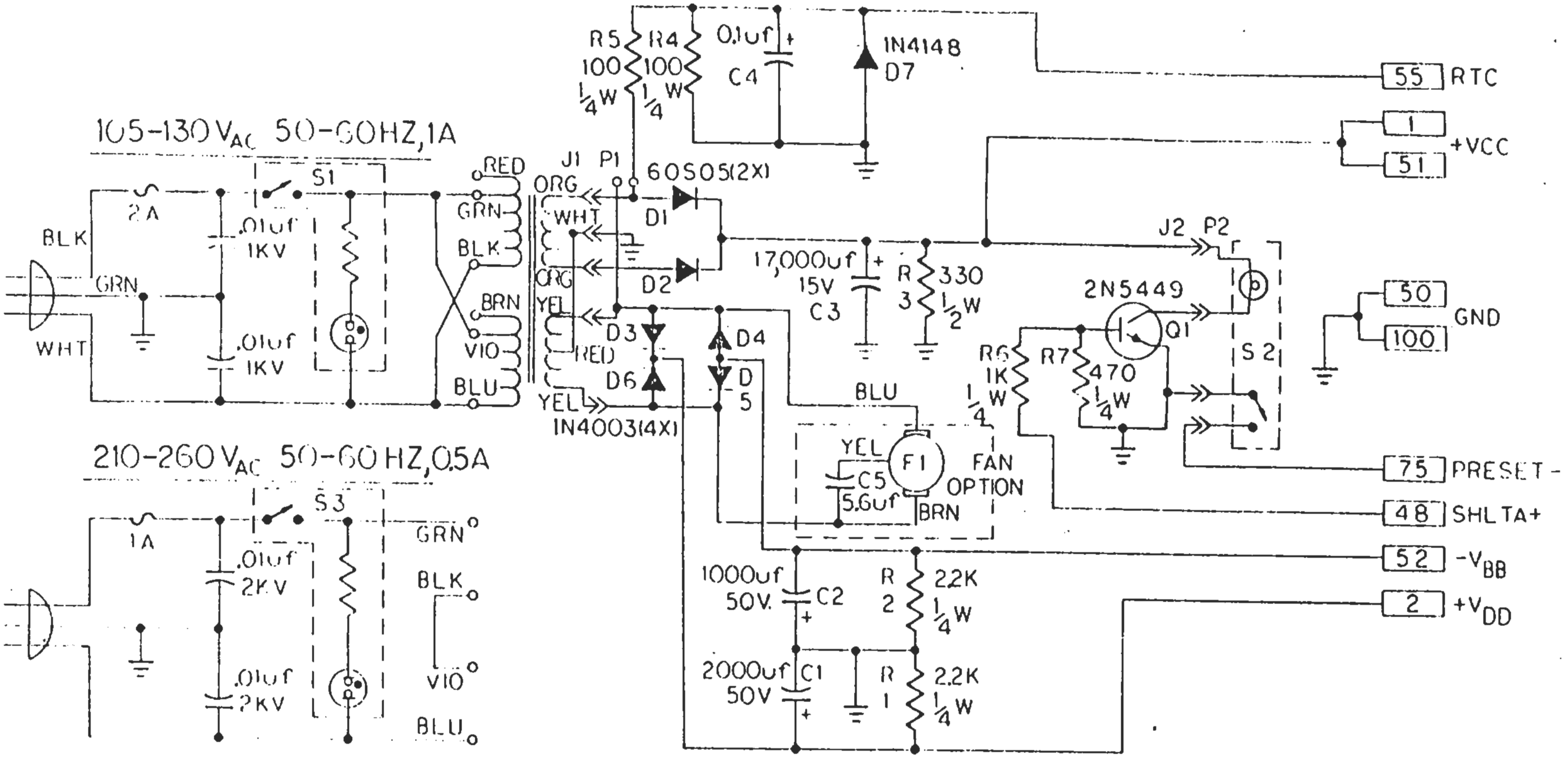
Single-step logic provides for causing an interrupt two instruction cycles after the logic has been enabled. Single-step logic is enabled by issuing an OUT C hex through OUT F hex instruction. PS3 and WR- are ANDed together in IC 37 and used to reset flip-flop IC 38. This causes $\overline{Q}$ output to go high, enabling IC 41. Input to the first section of IC 41 consists of clock signal SSTB- and a signal off the bus, D5. If SSTB- occurs while D6 is high, then the left-hand flip-flop of IC 41 will toggle, causing $\overline{Q}$ to go low. The next occurrence will cause $\overline{Q}$ to go high, creating a positive edge on the clock input to the right-hand flip-flop of IC 41. This will cause IC 41 to be set, generating an interrupt. During the interrupt acknowledge cycle, INTA+ will be true. This signal is applied to the J input of IC 38. This flip-flop is clocked by DBIN-. On the rising edge of DBIN-, and if J is high (at the end of the interrupt acknowledge cycle), IC 38 will be set, causing $\overline{Q}$ to return low, which in turn resets IC 41, which in its turn clears the interrupt.

While IC 38 is reset, other interrupts are inhibited. In order to inhibit interrupts, the $\overline{Q}$ output of IC 38 is tied to the $\overline{\text{enable}}$ of IC 2, the priority encoder. The interrupts from this encoder and the interrupt logic are ORed together in IC 40 and applied to the interrupt input on the CPU.

Bus Request Logic

Bus request logic uses ICs 10, 20, 19, 11, and 12. To generate a bus request, ONBD- must be high. ONBD- is ANDed with SSTB+, pin 4 of IC 12, in IC 20, and is used to set the flip-flop, pin 11 of IC 10. This causes $\overline{Q}$, pin 9 of IC 10, to go low, generating a bus request. The bus request is cleared at the end of the memory cycle when WR- goes high (if a write cycle) or when DBIN- goes high (if a read cycle). These two signals are ANDed together in IC 19 and applied to the clock input of IC 10, causing a Ø to be read into IC 10, which causes $\overline{Q}$ to go high. IC 10 may also be reset by POC+ or HLTA+. These two are ORed together in IC 11 and applied to pin 15 of IC 10.

APPENDICES



NOTES:

1. FOR HIGH LINE VOLTAGE OR IN SMALL SYSTEMS USE RED AND BRN TAPS INSTEAD OF GRN AND VIO, RESPECTIVELY.
2. ALL RESITANCE VALUES ARE IN OHMS.

QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION

PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

MATERIAL

FINISH

DO NOT SCALE DRAWING

NEXT ASSY | USED ON

APPLICATION

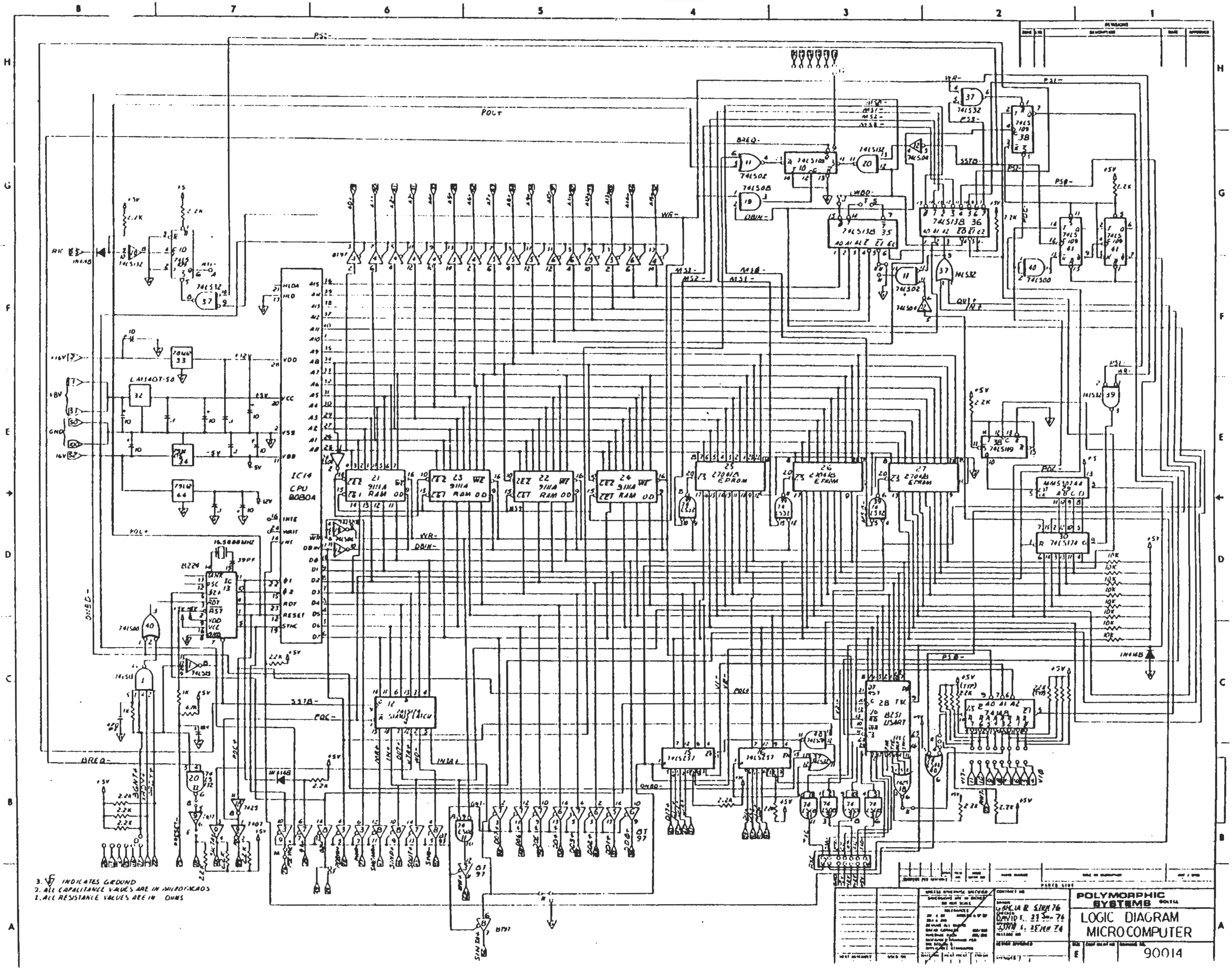
CONTRACT NO.

APPROVALS	DATE
DRAWN DAVID Forrester	10/11/76
CHECKED	

SCHEMATIC DIAGRAM POLY-88 POWER SUPPLY

SIZE	CODE IDENT NO.	DRAWING NO.
C		90021

SCALE SHEET / OF /



3. ⏚ INDICATES GROUND
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS
1. ALL RESISTANCE VALUES ARE IN OHMS

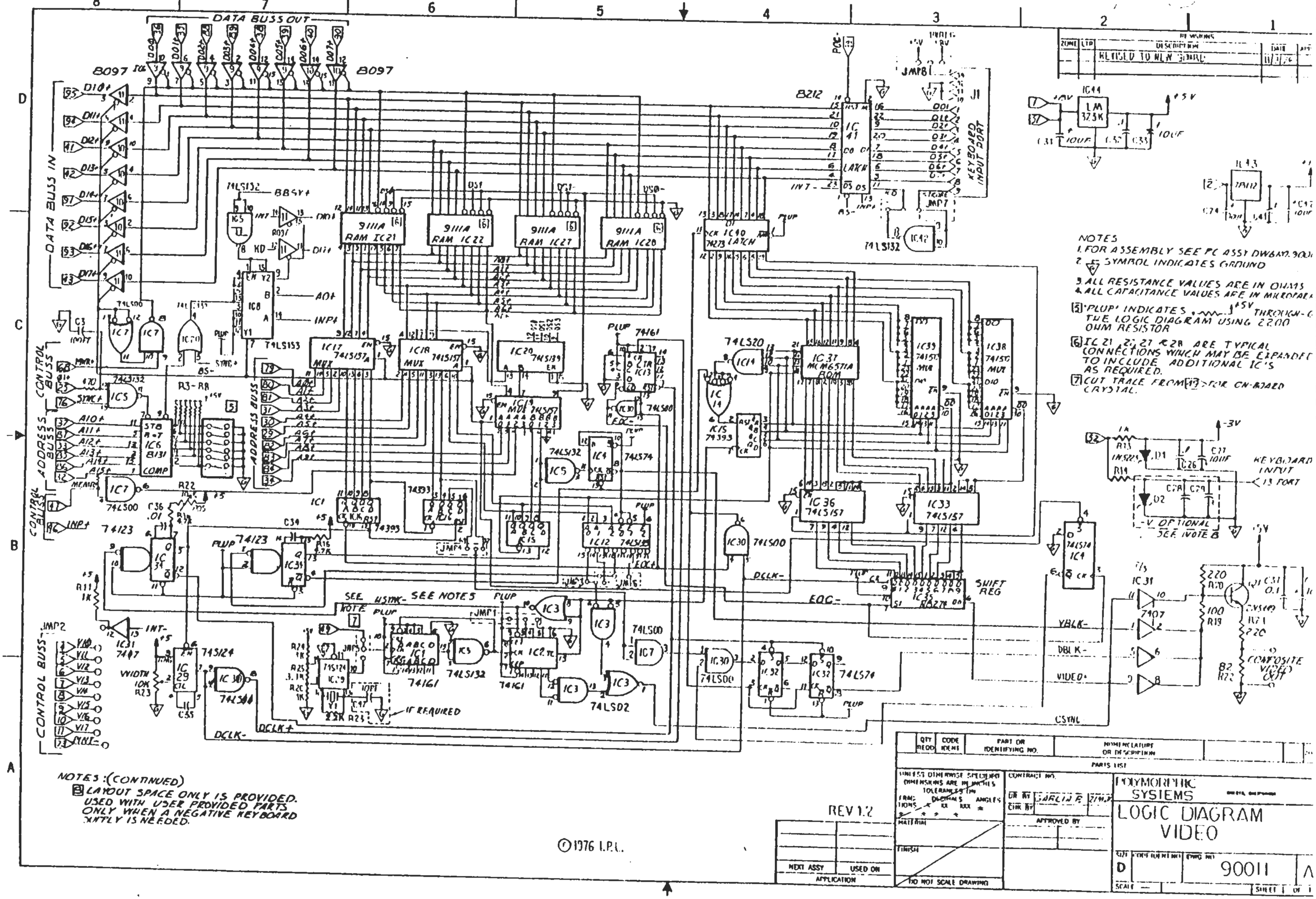
POLYMORPHIC SYSTEMS GOLETA

LOGIC DIAGRAM
MICROCOMPUTER

GARCIA R 5 JUN 76
DAVID L 23 JUN 76
JOHN E 25 JUN 76

E

90014



NOTES
1. FOR ASSEMBLY SEE PC ASSY DWG NO. 900
2. SYMBOL INDICATES GROUND
3. ALL RESISTANCE VALUES ARE IN OHMS
4. ALL CAPACITANCE VALUES ARE IN MICROFARA
[5] 'PLUP' INDICATES +5V THROUGH-O THE LOGIC DIAGRAM USING 2200 OHM RESISTOR
[6] IC 21, 22, 27 & 28 ARE TYPICAL CONNECTIONS WHICH MAY BE EXPANDEC TO INCLUDE ADDITIONAL IC'S AS REQUIRED.
[7] CUT TRACE FROM [13] > FOR ON-BOARD CRYSTAL.

NOTES: (CONTINUED)
[8] LAYOUT SPACE ONLY IS PROVIDED. USED WITH USER PROVIDED PARTS ONLY WHEN A NEGATIVE KEYBOARD SUPPLY IS NEEDED.

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REV 1.2

ZONE	LTR	DESCRIPTION	DATE
		REVISED TO NEW BOARD	11/1/76

	QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION

PARTS LIST

NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON FRACTIONS DECIMALS .XX .XXX ANGLES

MATERIAL

FINISH

DO NOT SCALE DRAWING

CONTRACT NO.

DR BY GARCIA R. 2/11/7

CHK BY

APPROVED BY

POLYMORPHIC SYSTEMS

LOGIC DIAGRAM VIDEO

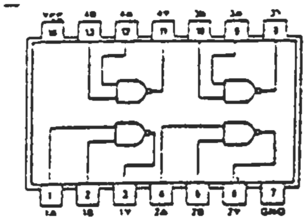
SIZE D

DWG NO 90011 A

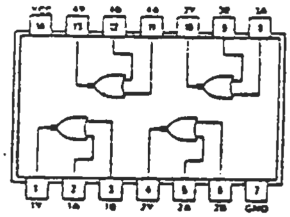
SCALE —

SHEET 1 OF 1

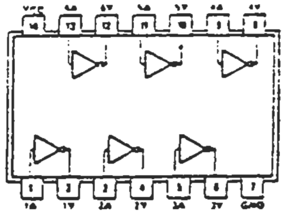
APPENDIX B: Chip pinouts



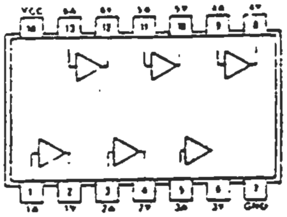
SN5400/SN7400(J, N)
SN54H00/SN74H00(J, N)
SN54L00/SN74L00(J, N)
SN54LS00/SN74LS00(J, N, W)
SN54S00/SN74S00(J, N, W)



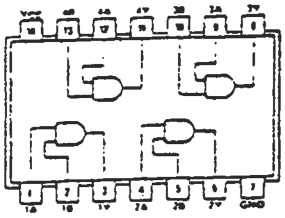
SN5402/SN7402(J, N)
SN54L02/SN74L02(J, N)
SN54LS02/SN74LS02(J, N, W)
SN54S02/SN74S02(J, N, W)



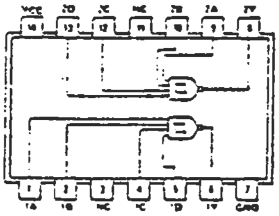
SN5404/SN7404(J, N)
SN54H04/SN74H04(J, N)
SN54L04/SN74L04(J, N)
SN54LS04/SN74LS04(J, N, W)
SN54S04/SN74S04(J, N, W)



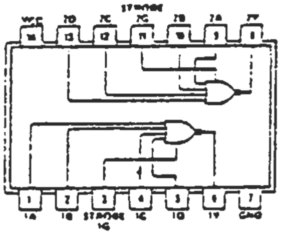
SN5407/SN7407(J, N, W)



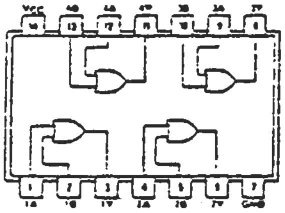
SN5408/SN7408(J, N, W)
SN54LS08/SN74LS08(J, N, W)



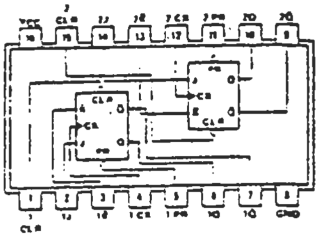
SN5413/SN7413(J, N, W)



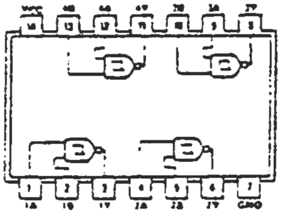
SN5425/SN7425 (J, N, W)



SN5432/SN7432(J, N, W)
SN54LS32/SN74LS32(J, N, W)

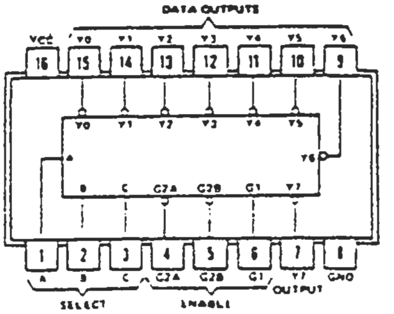


SN54109/SN74109(J, N, W)
SN54LS109/SN74LS109(J, N, W)



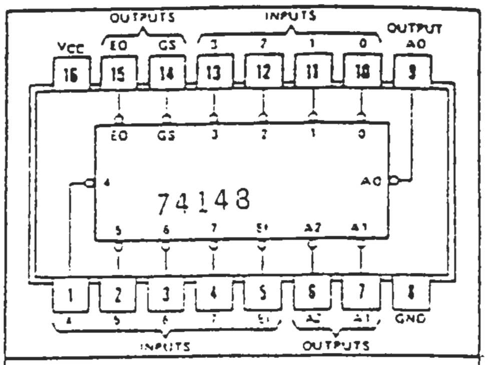
SN54132/SN74132(J, N, W)
SN54S132/SN74S132(J, N, W)

'LS138, 'S138
J OR N DUAL-IN-LINE OR
W FLAT PACKAGE (TOP VIEW)



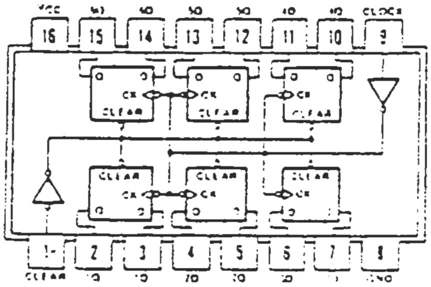
positive logic: see function table

J OR N DUAL-IN-LINE OR
W FLAT PACKAGE (TOP VIEW)

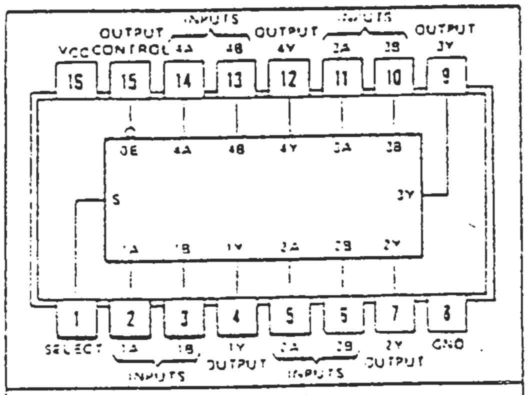


positive logic: see function table

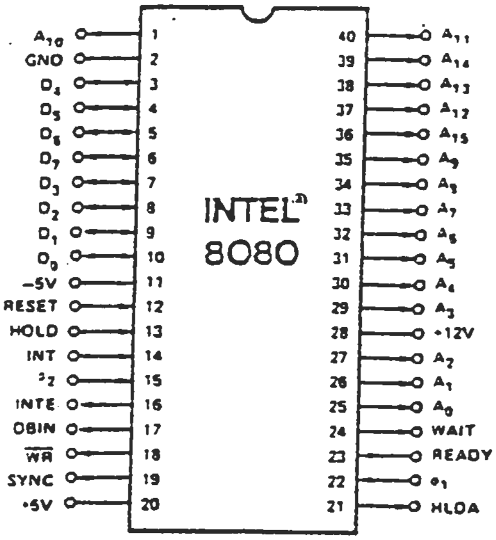
SN54S174 . . . J OR W PACKAGE
'174, 'LS174, SN74S174 . . . J, N, OR W PACKAGE
(TOP VIEW)

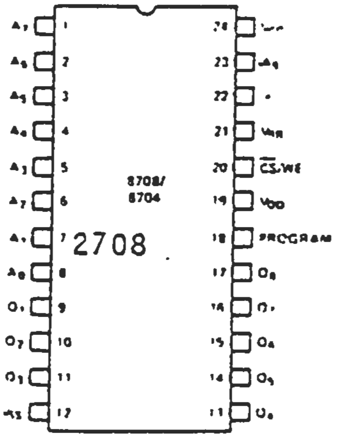


J OR N DUAL-IN-LINE OR W FLAT PACKAGE (TOP VIEW)
SN54S257, SN74S257

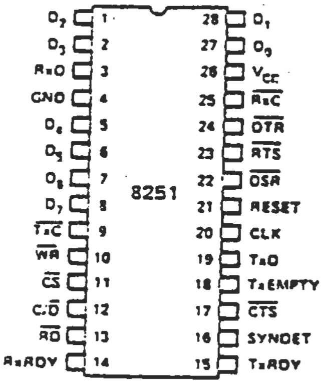


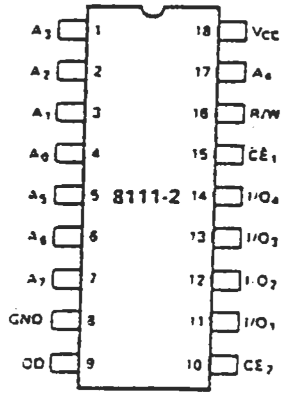
positive logic: see function table



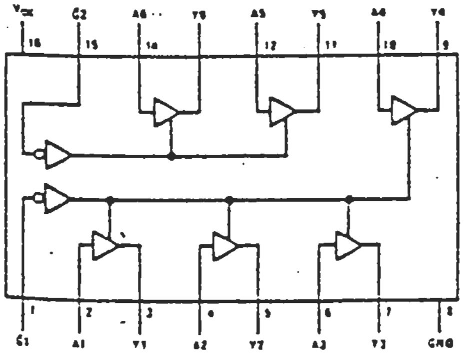


*8704 = VSS
8708 = A9



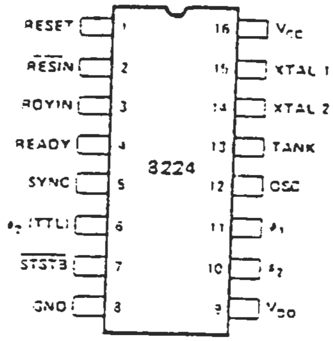


91L11

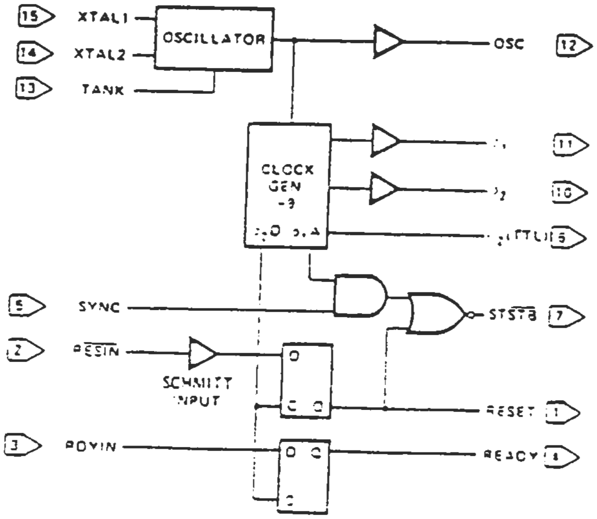


7097(J), (W); 8097(J), (N), (W);
70L97/80L97(J), (N), (W)

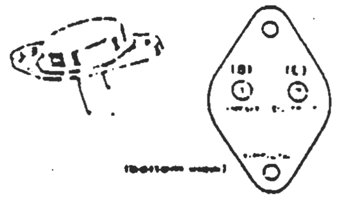
PIN CONFIGURATION



BLOCK DIAGRAM



POSITIVE
VOLTAGE REGULATOR
MONOLITHIC SILICON
INTEGRATED CIRCUIT



K SUFFIX
METAL PACKAGE
CASE 11
(TO-3 Type)

CASE 199-04
(P Suffix)

CASE 79-02
TO-39
(G Suffix)

POSITIVE, 500 mA – MC78M00 Series

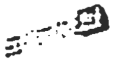
Family Characteristics
0 to +175°C Junction Temperature
I_O – 500 mA (Max)
V_O – ±5% of nominal voltage for all line and load condition limits

Nominal	V_I (dc)		
V_O	Min	Max	Device Type
5 V	7 V	35 V	MC78M05C
6 V	8 V	35 V	MC78M06C
8 V	10.5 V	35 V	MC78M08C
12 V	14.5 V	35 V	MC78M12C
15 V	17.5 V	35 V	MC78M15C
18 V	21 V	35 V	MC78M18C
24 V	27 V	40 V	MC78M24C

NEGATIVE, 100 mA – MC79L00 Series

Family Characteristics
0 to +175°C Junction Temperature
I_O – 100 mA (Max)
V_O – ±10% of nominal voltage for all line and load condition limits

Nominal	V_I (dc)		
V_O	Min	Max	Device Type
3 V	5 V	30 V	MC79L03C
5 V	7 V	30 V	MC79L05C
12 V	14.5 V	35 V	MC79L12C
15 V	17.5 V	35 V	MC79L15C
18 V	21 V	35 V	MC79L18C
24 V	27 V	40 V	MC79L24C



*CASE 29-02
TO-92
(P Suffix)

CASE 79-02
TO-39
(G Suffix)

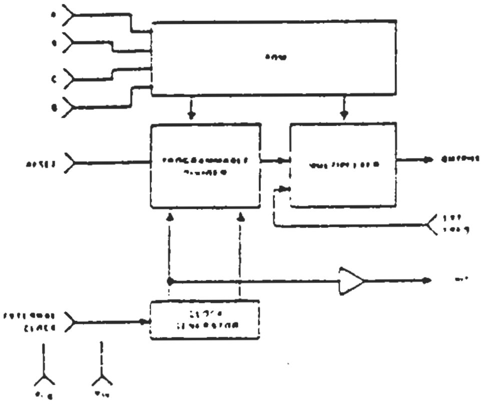
CASE 199-04
(P Suffix)

CASE 11
(K Suffix)

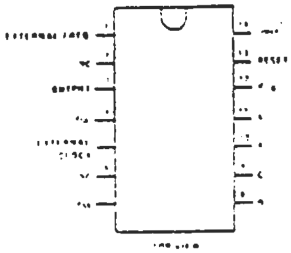
NEGATIVE, 1.5 A – MC7900 Series

Family Characteristics
0 to +175°C Junction Temperature
I_O – 1.5 A (Max)
V_O – ±5% of nominal voltage for all line and load condition limits

Nominal	V_I (dc)		
V_O	Min	Max	Device Type
2 V	7.2 V	35 V	MC7902C
5 V	7 V	35 V	MC7905C
5.2 V	7 V	35 V	MC7905.2C
6 V	8 V	35 V	MC7906C
8 V	10.5 V	35 V	MC7908C
12 V	14.5 V	35 V	MC7912C
15 V	17.5 V	35 V	MC7915C
18 V	21 V	35 V	MC7918C
24 V	27 V	40 V	MC7924C



Dual In-Line Package

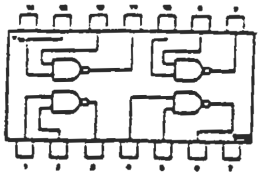


Order Number MM5307 AA/D
See Package 2

Order Number MM5307AA/N
See Package 14

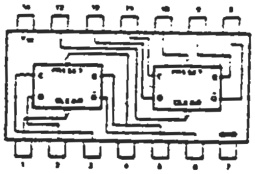
A,F PACKAGE

7400

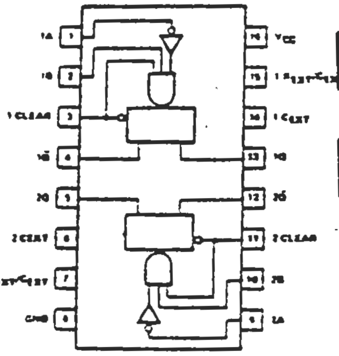


A,F PACKAGE

7474

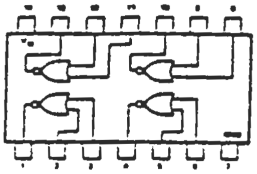


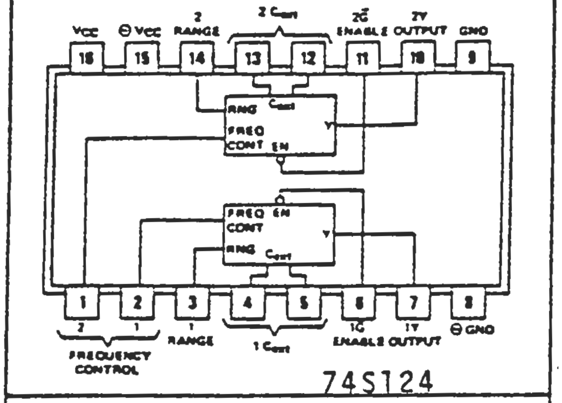
74123



A,F PACKAGE

7402



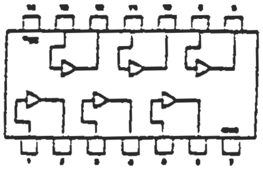


74S124

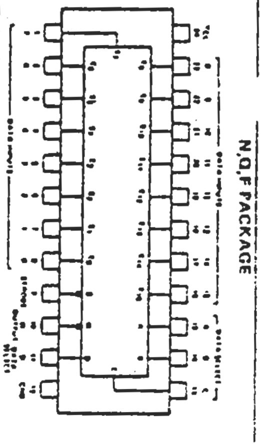
positive logic: While the enable input is low, the output is enabled. While the enable input is high, the output is high.

A,F PACKAGE

7407

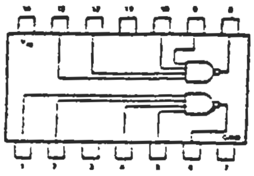


74150

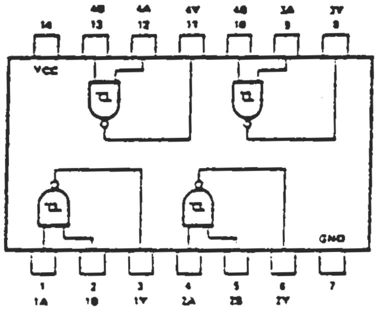


A,F PACKAGE

7420

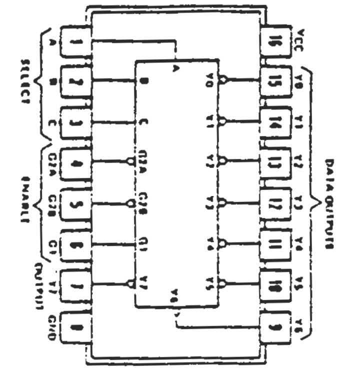


S54132, N74132



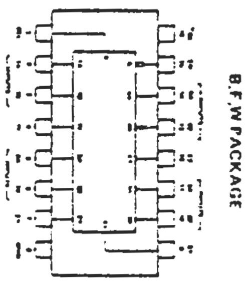
POSITIVE LOGIC: $Y=\overline{AB}$

74LS138

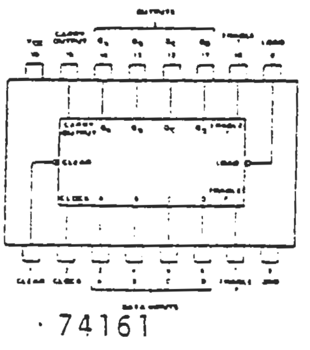


positive logic: see function table

74157

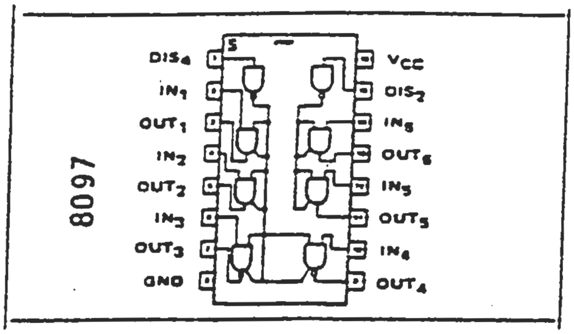


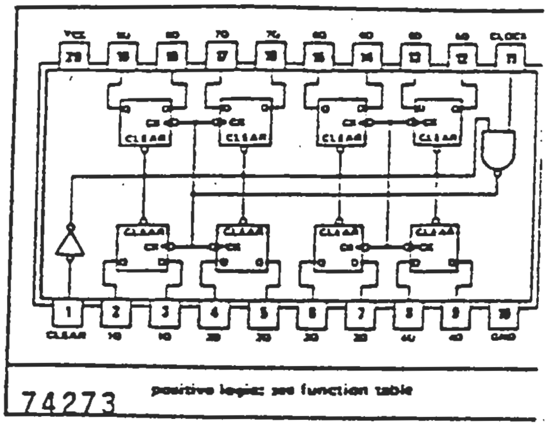
B,F,W PACKAGE



· 74161

APPENDIX B: Chip pinouts

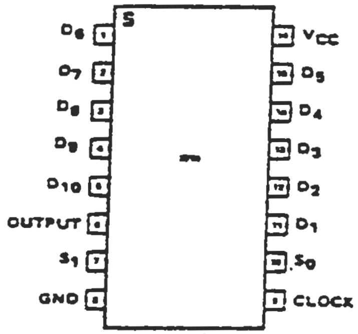




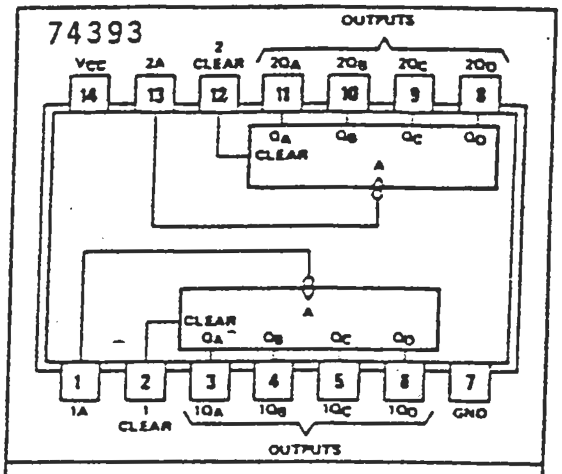
74273

positive logic: see function table

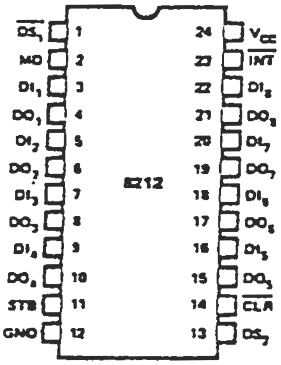
N8274B

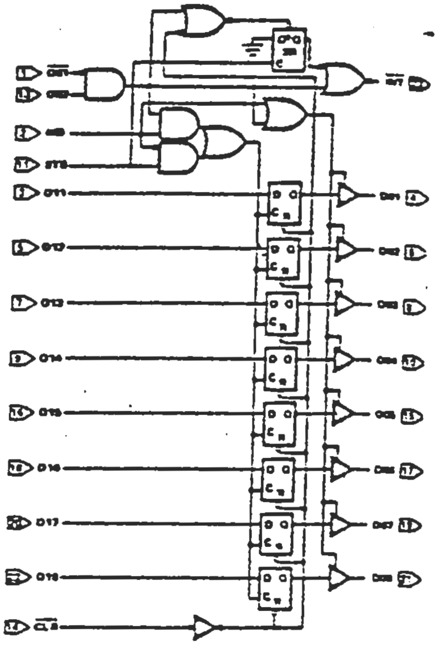


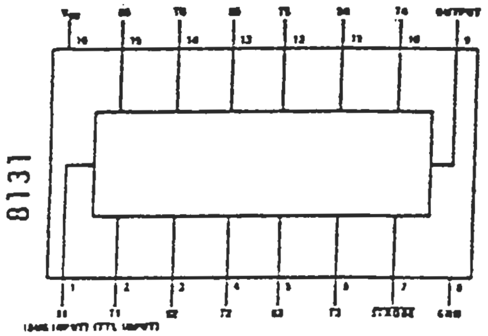
74393



positive logic: High input to clear resets all four outputs low

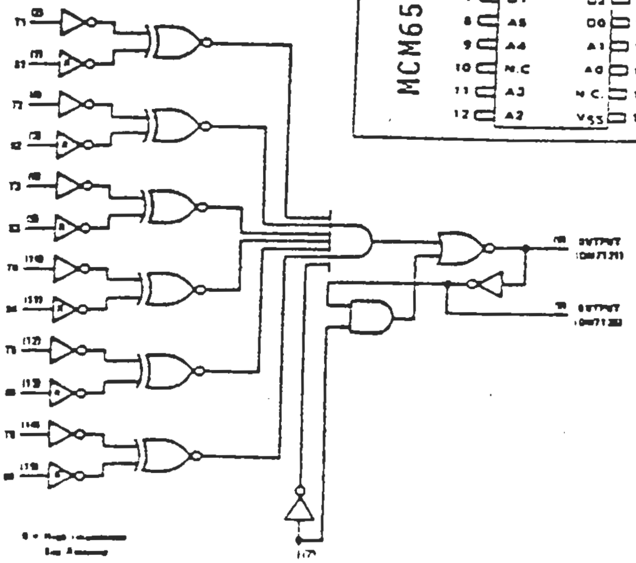






7131(J), (W); 8131(J), (N), (W);
7136(J), (W); 8136(J), (N), (W)

Logic Diagram

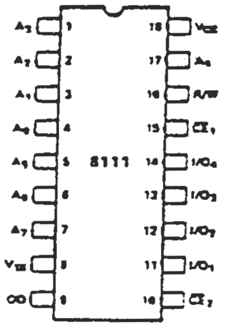


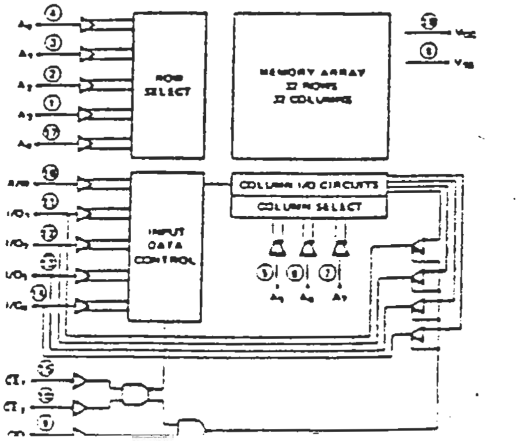
MCM657x

PIN ASSIGNMENT

1	VBB	RS3	24
2	VCC	RS2	23
3	VDD	RS1	22
4	A6	RS0	21
5	D5	D6	20
6	D3	D4	19
7	D1	D2	18
8	A5	D0	17
9	A4	A1	16
10	N.C	A0	15
11	A3	N.C.	14
12	A2	VSS	13

2111





Memory Functions of the Poly 88 CPU

1.1 Introduction

Memory external to the CPU board is normally quite simple to use. Memory cards simply plug into the POLY 88 bus after you have selected an appropriate starting address. One exception is the block of memory between addresses ØØØØ hex and ØFFF hex; the CPU disregards any external memory at this address unless you have made the appropriate modification.

1.2 External lower memory.

The CPU hardware modifications necessary for use of a second block of memory at lower addresses is fairly simple, as it was considered when the board was designed. Some memory cards (including those manufactured by PolyMorphic Systems) have "phantom" capabilities on bus pin 67. These offer an advantage when making this modification but are not necessary in many cases. The POLY 88 monitor PROM will be disabled; so some software additions will be necessary. The software additions can be lengthy or short depending on your particular application.

1.3 Hardware changes for external lower memory.

As a general rule, make sure the normal functions of the system are operational before attempting any special alterations. Cut trace "HH" and remove a small section. This trace is near the upper left corner of the CPU board when viewing the bottom (non-component side). Install a jumper (on the non-component side of the board) between the pad at the right end of the trace "HH" (ungrounded pad) and pad "H" directly above capacitor C9. Pad "H" is labeled only on the component side. Two pads are provided so you can use a jumper to replace trace "HH" if it becomes necessary.

If the memory card you will use as a second block of lower memory has a "phantom" facility at bus pin 67, connect a jumper between bus pin 67 and pin 6 of IC12, on the non-component side of the CPU board. Bus pin 67 has a jumper pad attached, pin 6 of IC12 does not have a jumper pad.

Be sure to double check the connections you make before applying power; misplaced jumpers are a common source of serious damage to integrated circuits.

1.4 Theory behind hardware changes.

IC35 is a 74LS138 3-line to 8-line decoder. Address lines A13 through A15 are decoded by this chip to porduce a LO TTL level signal at one of its outputs. A12 is connected to an active-LO enable input of IC35, thus the chip can produce a LO output only when A12 is LO. When all four address lines are LO (indicating the first 4K of memory), the output at IC35 pin 15 is LO creating an active onboard signal (ONBD-). One function of ONBD- is to provide an enable to IC36, another 3-line to 8-line decoder. IC36 is completely enabled when ONBD- and INTA+ (interrupt acknowledge) are both LO. At this time, address lines A1Ø and A11 are decoded to select 1K of onboard memory (memory select signals = MSØ- through MS3-) or one of four onboard I/O signals (peripheral select signals = PSØ- through PS3-).

The output of IC37 pin 3 determines whether memory blocks or I/O signals are decoded. The output of IC37 pin 3 is HI if an input or output instruction is being executed.

Returning to the discussion of IC35, notice the enable at pin 5 (active LO) is normally grounded through trace "HH". If trace "HH" is broken and pin 5 is connected to pad "H", IC35 is enabled only when A12 and output pin 13 of IC11 are both LO. IC11 pin 13 goes LO when the output of IC37 to pin 3 is LO (indicating neither input nor output instructions are being performed) and IC30 pin 7 is HI.

IC30 is used as a latch to store baud rate, serial device select, and onboard disable status; it will be referred to by the name BRG (baud rate generator latch) for ease of discussion. The BRG output pins continually display the aforementioned status according to Figure 1.

To disable the onboard memory, set bit 5 (of bits Ø through 7) HI in the accumulator and output to port 4 (BRG).

```
          Example: MVI A,2ØH; SET BIT 5 HI
                   OUT 4    ; LATCH NEW STATUS IN BRG
```

To re-enable the onboard memory set bit 5 of port 4 LO or press the front panel reset button. The latter resets the BRG and executes the monitor which places a given status in the BRG.

The other hardware change suggested for memory cards having a "phantom" facility enables the memory card when pin 7 of BRG is HI (onboard memory disable) and disables the memory card when pin 7 is LO (assuming bus pin 67 disables the memory card when HI). The "phantom" facility is not absolutely necessary but without it, writing into onboard memory (including stack ops performed by the monitor) also writes into the corresponding offboard memory location.

Remember, when the onboard memory is disabled, the POLY 88 monitor ROM is disabled. Thus, you must have any necessary control software (such as keyboard input, video display, and cassette tape reader routines) located in memory external to the CPU board.

1.5 Relocation of CPU onboard memory.

The onboard memory address can be shifted up if you do not wish to use the POLY 88 monitor ROM. It is important to remember the POLY 88 monitor will work only if its starting address is ØØØØ.

There are three possible starting addresses that are easily implemented on the POLY 88 CPU, ØØØØ (which is preselected on the PC card), 8ØØØ hex (32K), and EØØØ (56K). If you wish to select a starting location other than ØØØØ, cut trace "J" and remove a small section. Trace "J" is between two closely spaced pads on the non-component side, immediately to the right of IC35. Install a jumper with sleeving between pad "J" (the one nearest the regulators) and pad "R" (which connects to IC35 pin 14 and is labeled "T" in the schematic) for a starting location of 3ØØØ hex; install a jumper between pad "J" (nearest the regulators) and pad "S"(connects to IC35 pin 7) for a starting location of EØØØ hex.

These changes simply create the ONBD- signal when the new memory block address is decoded by IC35.

Figure 1

D5/7	D4/15	D3/2	D2/12	D1/10	DØ/5	ONBD	SERIAL DEVICE	IC29 OUTPUT KHZ	÷16 BAUD RATE
L	X	X	X	X	X	E	X	X	X
H	X	X	X	X	X	D	X	X	X
X	L	X	X	X	X	X	Ø	X	X
X	H	X	X	X	X	X	1	X	X
X	X	L	L	L	L	X	X	0	0
X	X	L	L	L	H	X	X	0.800	50
X	X	L	L	H	L	X	X	1.200	75
X	X	L	L	H	H	X	X	1.760	110
X	X	L	H	L	L	X	X	2.152	134.5
X	X	L	H	L	H	X	X	2.400	150
X	X	L	H	H	L	X	X	4.800	300
X	X	L	H	H	H	X	X	9.600	600
X	X	H	L	L	L	X	X	14.400	900
X	X	H	L	L	H	X	X	19.200	1200
X	X	H	L	H	L	X	X	28.800	1800
X	X	H	L	H	H	X	X	38.400	2400
X	X	H	H	L	L	X	X	57.600	3600
X	X	H	H	L	H	X	X	76.800	4800
X	X	H	H	H	L	X	X	115.20	7200
X	X	H	H	H	H	X	X	153.60	9600

H = TTL HI   L = TTL LO   X = Irrelevant

E = Enabled   D = Disabled

D5/7 means the status bit latched from data line D5 and output from BRG pin 7.

DIFFERENCES BETWEEN POLY 88 BUS AND ALTAIR 8800 OR IMSAI 8080 BUS

Front-panel Control Signals - a number of signals generated or used by the Altair/Imsai front panel are not used by the POLY 88 system. These include 21(UNPROT), 22(SS), 53(SSWI-), 54(EXTCLR), 56(STSTB), 57(FRDY), 69(PS-), 7Ø(PROT), and 71(RUN).

Status Signals - Four status signals defined in the Altair/Imsai bus are not present in the POLY 88. The SSTACK (98) signal is not generated and the SM1(44) signal is used only internally on the processor card. The PWAIT (pin 27) and PINTE (pin 28) signal are not brought out to the bus but are available as test points on the CPU card.

DMA Control Signals - In the POLY 88 system the DMA (direct memory access) is not controlled as in the Altair or IMSAI. The POLY 88 CPU may continue processing during DMA cycles by using it onboard memory and I/O. This also allows more than one processor card to share a common bus (backplane) with little conflict.

Bus contention for DMA and multiprocessing is handled by the DMA/multiprocessing controller card. The control lines defined in the Altair/Imsai may be used but go to the controller and are not present on the CPU card. Pins 18 (STAT DSB-), 19(C/S DSB-), 22 (ADDR DSB-), 23 (DO DSB-), 26 (PHLDA), and 74 (PHOLD-) are affected.

POLY-88 BUS

1	+8V	Unregulated voltage, regulated to +5V on ca
2	+16V	Unregulated voltage, regulated to +12V on c
3	XRDY+	External ready--ready input to CPU
4	VIØ-	Vectored interrupt line
5	VI1-	Vectored interrupt line
6	VI2-	Vectored interrupt line
7	VI3-	Vectored interrupt line
8	VI4-	Vectored interrupt line
9	VI5-	Vectored interrupt line
10	VI6-	Vectored interrupt line
11	VI7-	Vectored interrupt line
12	XRDY2	External ready 2
13	--	Reserved for bus control
14	--	Reserved for bus control
15	--	Reserved for bus control
16	--	Reserved for bus control
17	--	Reserved for bus control
18	--	Reserved for bus control
19	--	Reserved for bus control
20	--	Unused
21	--	Unused
22	--	Reserved for bus control
23	--	Reserved for bus control
24	Ø2+	Phase 2 clock from CPU

25	Ø1+	Phase 1 clock from CPU
26	--	Reserved for bus control
27	--	Unused
28	--	Unused
29	A5+	Address line
30	A4+	Address line
31	A3+	Address line
32	A15+	Address line
33	A12+	Address line
34	A9+	Address line
35	DO1+	Data out line
36	DOØ+	Data out line
37	A1Ø+	Address line
38	DO4+	Data out line
39	DO5+	Data out line
40	DO6+	Data out line
41	DI2+	Data in line
42	DI3+	Data in line
43	DI7+	Data in line
44	--	Unused
45	SOUT+	Output -- during this machine data is transferred from the C to an output port.
46	SINP+	Input -- during this machine c data is transferred from an inpu port to CPU.
47	SMEMR+	Memory read cycle
48	SHLTA+	Halt -- CPU has entered a halt
49	CLOCK-	Phase 2 clock
50	GND	System ground

51	+8V	Unregulated voltage regulated on card to
52	-16V	Unregulated coltage regulated on card to or -5V
53	--	Unused
54	--	Unused
55	RTC+	Real time clock--half wave rectified 5Ø/6 Hz signal
56	--	Unused
57	--	Unused
58	--	Unused
59	--	Reserved
60	--	Reserved
61	--	Reserved
62	--	Reserved
63	--	Reserved for MP/DMA controller
64	--	Reserved for MP/DMA controller
65	--	Reserved for MP/DMA controller
66	--	Reserved for MP/DMA controller
67	PHANTOM-	Used to disable RAM and I/O addressing
68	MWRTTE+	Memory--write strobe for memory cycle
69	--	Unused
70	--	Unused
71	--	Unused
72	PRDY+	Processor ready--ready input to CPU
73	PINT-	Processor Interrupt--used only with external interrupt controller
74	--	Reserved for bus control
75	PRESET-	Reset--from front bus control panel pus button--set PC to Ø

76	PSYNC+	Sync--identifies beginning of machine c
77	PWR-	Write--CPU write strobe
78	PDBIN+	Data in--CPU read strobe
79	AØ+	Address line
80	A1+	Address line
81	A2+	Address line
82	A6+	Address line
83	A7+	Address line
84	A8+	Address line
85	A13+	Address line
86	A14+	Address line
87	A11+	Address line
88	DO2+	Data out line
89	DO3+	Data out line
90	DO7+	Data out line
91	DI4+	Data in line
92	DI5+	Data in line
93	DI6+	Data in line
94	DI1+	Data in line
95	DIØ+	Data in line
96	SINTA+	Interrupt acknowledge cycle
97	SWO-	Write/output--machine cycle to write to memory or output to port
98	--	Unused
99	POC-	Power on clear--generated by PRESET+ o turn on used to reset CPU and I/O device
100	GND	System ground

MEMORY ADDRESSING, VECTORED INTERRUPT,
AND SERIAL I/O

Memory and I/O Addressing The CPU/8 processor card may contain up to 3.5K bytes of onboard RAM and ROM. This memory occupies a contiguous 4K address space which is jumper selectable to start at Ø, 8ØØØH, or EØØØH (see Figure 1). The CPU/8 board is shipped prewired to start at address Ø. This may be modified by removing jumper "J" and replacing it with jumpers from J to S or J to T. The onboard I/O port address space follows the onboard memory address space as shown in Figure 1.

Space for three 2708 UV erasable PROM's or three 2308 masked ROM'S is provided on the CPU/8. The ROM's occupy the first 3K bytes of the 4K address space. Also provided on the CPU/8 is 512 bytes of read/write memory (RAM). This RAM occupies the upper 1K of address space. Figure 1 shows to ½K block of RAM. These are in fact the same ½K block of RAM as the address of each cell is not unique. Two addresses exist for each byte of RAM. Address D7FH contains the same information as address F7FH. This is caused by the fact that address bit 8 is not decoded when addressing onboard RAM.

USART and Baud Rate Latch The use of the USART and baud rate latch is discussed in a separate section "Programming the SER/8 serial option."

Real-Time Clock The real-time clock (RTC) circuit generates and interrupts for every positive going edge of the 50Hz or 60 Hz line frequency. This interrupt is latched and remains on until it is reset by issuing an output command to the real-time clock port. It is the programmer's responsibility to reset the RTC, before reenabling interrupts, when he services the clock. This is done by doing an OUT 8, OUT 88H or OUT ØE8H instruction depending upon the location of the onboard ports. Vectored interrupt 1 (trap address 3ØH) is generally used for the real-time clock interrupt service routine. The real-time clock is physically connected on the CPU board by a jumper from the RTC pad in the upper left hand side of the board to VT1 in the interrupt jumper area.

Single-Step Logic The single step logic hardware uses vectored interrupt Ø for the purpose of executing a single instruction of a program being tested and returning to a fixed location (38H) in RAM. Issuing an output instruction to the single-step port causes the single step logic to be enabled. This also causes all other interrupts to be disabled (masked). The logic will count out 2 instruction cycles and then generate an interrupt which is vectored to location 38H. The single-step logic is immediately reset and its interrupts that were masked off are unmasked. Note that it is still not possible to be interrupted until an enable interrupt (EI) instruction is executed.

The two instructions normally executed after the output instruction are a return (to the program bring single-stepped) and one instruction out of the program being single-stepped. For an example of the use of the single-step logic see the assembly listing for the POLY 88 resident monitor.

Using the vectored interrupts The 8 vectored interrupt traps in the 8080A CPU chip are located every 8 bytes in the first 64 bytes of memory (see Figure 2). The first trap is also used by the reset function on the CPU so is generally not available for use as an interrupt. The last trap (38H) is used by the single-step logic on the CPU/8 card so it is also not available if the single-step function is to be used.

Consequently, only 6 (or 7) vectored interrupts are generally available. The 8 bytes at each trap location are usually not enough for the interrupt service routine, but are enough to save the state of the CPU and jump to the actual routine (see Figure 3).

The address of the service routines are stored in a table (ISRTBC) in RAM so that the service routines may be modified dynamically. The routine IORET restores the CPU registers and enables interrupts before returning to the interrupted program.

Power on reset When power is applied to the CPU a reset signal is generated for approximately ½ second. This causes the program counter to be reset to zero and the interrupts to be disabled. When this signal is released execution begins sequentially from location zero. The first 5 locations in memory (Ø to 4) are generally used for a portion of the cold-start routine and a jump in the next 3 (5-7) jumps to the rest of the cold start routine (see POLY 88 resident monitor). This is done because location 8 is generally used for vectored interrupt 6.

CPU/8 I/O ADDRESSING

Address (Hex)*			R/W	Function
J	S	T		
Ø,2	8Ø,82	EØ,E2	R	USART status byte
Ø,2	8Ø,82	EØ,E2	W	USART command/node
1,3	81,83	E1,E3	R	USART received data
1,3	81,83	E1,E3	W	USART transmit data
4-7	84-87	E4-E7	R	Unused
4-7	84-87	E4-E7	W	Baud Rate Latch
8-B	88-8B	E8-EB	R	Unused
8-B	88-8B	E8-EB	W	Reset real-time clock
C-F	8C-8F	EC-EF	R	Unused
C-F	8C-8F	EC-EF	W	Start single step

CPU/8 MEMORY ADDRESSING

Address*			Function
J	S	T	
Ø-3FF	8ØØØ-83FF	EØØØ-E3FF	ROM #1
4ØØ-7FF	84ØØ-87FF	E4ØØ-E7FF	ROM #2
8ØØ-BFF	88ØØ-8BFF	E8ØØ-EBFF	ROM #3
CØØ-DFF	8CØØ-8DFF	ECØØ-EDFF	Onboard RAM
EØØ-FFF	8EØØ-8FFF	EEØØ-EFFF	Onboard RAM **

* Jumpers J, S and T determine the base address of the CPU memory and I/O address space

**This is the same RAM as the 512 bytes below it. (Bit 9 of the address is not decoded).

Figure 1

Vectored Interrupt Locations

Interrupt #	Address (Hex)
Ø	38*
1	3Ø
2	28
3	2Ø
4	18
5	1Ø
6	8
7	Ø**

* This location is also used for the single-step trap.

**This location is also used for the power-on reset.

Figure 2

INTRODUCTION

The SER/8 serial port option for the CPU/8 CPU card provides a very flexible serial communications interface for the POLY-88. The SER/8 provides a universal synchronous/asynchronous receiver/transmitter and a software controllable baud rate generator. The USART may interface to two serial I/O devices. The device and its baud rate may be changed under the control of one output port. These interface through two "minicards" which mount to the rear of the POLY-88 chassis. Interface cards are available for RS-232-C, current loop, Kansas City (Byte) Standard audio cassette, and the 1200 baud bi-phase cassette.

This note describes the SER/8 option from a functional standpoint and then describes the various operating modes of the USART and how the SER/8 may be programmed.

COMMUNICATIONS FORMATS

Serial communications, either on a data link or with a local peripheral, occurs in one of two basic formats; asynchronous or synchronous. These formats are similar in that they both require framing information to be added to the data to enable proper detection of the character at the receiving end. The major difference between the two formats is that the asynchronous format requires framing information to be added to each character, while the synchronous format adds framing information to blocks of data, or messages. Since the synchronous format is more efficient than the asynchronous format but requires more complex decoding it is typically found on high-speed data links, while the asynchronous format is used on lower speed lines.

The asynchronous format starts with the basic data bit to be transmitted and adds a "START" bit to the front of them and one or more "STOP" bits behind them as they are transmitted. The START bit is a logical zero, or SPACE, and is defined as the positive voltage level by RS-232-C. The STOP bit is a logical one, or

MARK, and is defined as the negative voltage level by RS-232-C. In current loop applications current flow normally indicates a MARK and lack of current a SPACE. The START bit tells the receiver to start assembling a character and allows the receiver to synchronize itself with the transmitter. Since this synchronization only has to last for the duration of the character (the next character will contain a new START bit), this method works quite well assuming a properly designed receiver. One or more STOP bits are added to the end of the character to ensure that the START bit of the next character will cause a transition on the communication line and to give the receiver time to "catch up" with the transmitter if its basic clock happens to be running slightly slower than the transmitter clock. If, on the other hand, the receiver clock happens to be running slightly faster than the transmitter clock, the receiver will perceive gaps between characters but will still correctly decode the data. Because of this tolerance to minor frequency deviations, it is not necessary that the transmitter and receiver clocks be locked to the identical frequency for successful asynchronous communication.

The synchronous format, instead of adding bits to each character, groups characters into records and adds framing characters to the record. The framing characters are generally known as SYN characters and are used by the receiver to determine where the character boundaries are in a string of bits. Since synchronization must be held over a fairly long stream of data, bit synchronization is normally either extracted from the communication channel by the modem or supplied from an external source.

An example of the synchronous and asynchronous formats is shown in Figure 1. The synchronous format shown is fairly typical in that it requires two SYN characters at the start of the message. The asynchronous format, also typical, requires a START bit preceding each character and a single STOP bit following it. In both cases, two 8-bit characters are to be transmitted. In the asynchronous mode 10 n bits are used to transmit n characters and in the synchronous mode 8n + 16 bits are used. For the example shown the asynchronous mode is actually more efficient, using 20 bits versus 32. To transmit a thousand characters in the asynchronous mode, however, take 10,000 bits versus 8,016 for the synchronous format mode. For long messages the synchronous format becomes much more efficient than the asynchronous format; the crossover point for the examples shown in Figure 1 is eight characters, for which both formats require 80 bits.

In addition to the differences in format between synchronous and asynchronous communication, there are differences with regards to the type of modems that can be used. Asynchronous modems typically employ FSK (Frequency Shift Keying) techniques which simply generate one audio tone for a MARK and another for a SPACE. The receiving modem detects these tones on the telephone line, converts them to logical signals, and presents them to the receiving terminal. Since the modem itself is not concerned with the transmission speed, it can handle baud rates from zero to its maximum speed. Synchronous modems, in contrast to asynchronous modems, supply timing information to the terminal and require data to be presented to them in synchronism with this timing information. Synchronous modems, because of this extra clocking, are only capable of operating at certain preset baud rates. The receiving mode, which has an oscillator running at the same frequency as the transmitting modem, phase locks its clock to that of the transmitter and interprets changes of phase as data. The PolyMorphic bi-phase cassette interface operates in a synchronous mode.

In some cases it is desirable to operate in a hybrid mode which involves transmitting data with the asynchronous format using a synchronous modem. This occurs when an increase in operating speed is required without a change in the basic protocol of the system. This hybrid technique is known as isosynchronous and involves the generation of the start and stop bits associated with the asynchronous format, while still using the modem clock for bit synchronization. The Byte standard cassette interface operates in an isosynchronous mode.

The 8251 USART (Universal Synchronous/Asynchronous Receiver) has been designed to meet a broad spectrum of requirements in the synchronous, asynchronous, and isosynchronous modes. In the synchronous modes it operates with 5, 6, 7, or 8-bit characters. Even or odd parity can be optionally appended and checked. Synchronization can be achieved internally via SYN character detection. SYN detection can be based on one or two characters which may or may not be the same. The single or double SYN characters are inserted into the data stream automatically if the software fails to supply data in time. The automatic generation of SYN characters is required to prevent the loss of synchronization. In the asynchronous mode the USART operates with the same data and parity structures as it does in the synchronous mode. In addition to appending a START bit to this data, it appends 1, 1½, or 2 STOP bits. Proper framing is checked by the receiver and a status flag set if an error occurs. In the asynchronous mode the USART can be programmed to accept clock rates of 1, 16, or 64 times the required baud rate. Note that X1 operation is only valid if the clocks of the receiver and transmitter are synchronized.

The USART can transmit the three formats in half or full duplex mode and is double-buffered internally (i.e., the software has a complete character time to respond to a service request). Although the USART supports basic data set control signals (e.g., DTR and RST), it does not fully support the signaling described in EIA RS-232-C. Examples of unsupported signals are Ring Indicator (CE), and the second channel signals. The serial option does not interface to the voltage levels required by EIA RS-232-C; this interface is provided by the SIO/2 card. (The SIO/2 also provides an optically isolated current loop interface).

A block diagram of the SER/8 serial port option is shown in Figure 2. As can be seen in the figure, the USART consists of five major sections which communicate with each other on an internal data bus. The five sections are the receiver, transmitter, modem control, read/write control, and I/O Buffer. In order to facilitate discussion, the I/O Buffer has been shown broken down into its three major subsections: the status buffer, the transmit data/command buffer, and the receive data buffer.

RECEIVER

The receiver accepts serial data on the RxD pin and converts it to parallel data according to the appropriate format. When the USART is in the asynchronous mode, and it is ready to accept a character (i.e., it is not in the process of receiving a character), it looks for a low level on the RxD line. When it sees the low level, it assumes that it is a START bit and enables an internal counter. At a count equivalent to one-half of a bit time, the RxD line is sampled again. If the line is still low, a valid START bit has probably been received and the USART proceeds to assemble the character. If the RxD line is high when it is sampled, then either a noise pulse has occured on the line or the receiver has become enabled in the middle of the transmission of a character. In either case the receiver aborts its operation and prepares itself to accept a new character. After the successful reception of a START bit the USART clocks in the data, parity, and STOP bits, and then transfers the data on the internal data bus to the receive data register. When operating with less than 8 bits, the characters are right-justified. The RxRDY signal is asserted to indicate that a character is available.

In the synchronous mode the receiver simply clocks in the specified number of data bits and transfers them to the receiver buffer register, setting RxRDY. Since the receiver blindly groups data bits into characters, there must be a means of synchronizing the receiver to the transmitter so that the proper character boundaries are maintained in the serial data stream. This synchronization is achieved in the HUNT mode.

In the HUNT mode the USART shifts in data on the RxD line one bit at a time. After each bit is received, the receiver register is

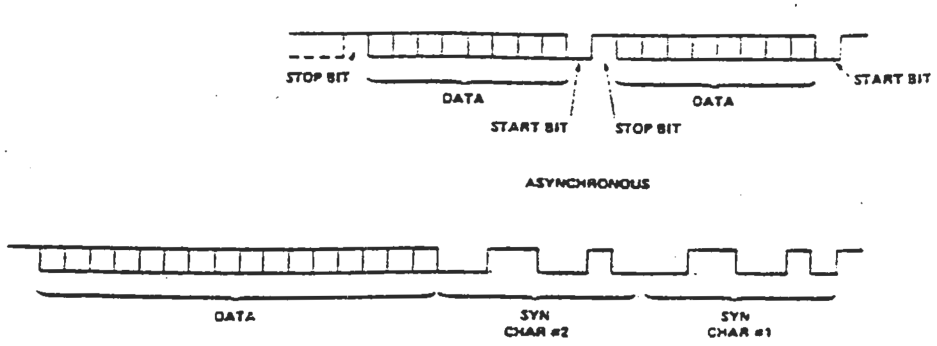


Figure 1. Transmission Formats

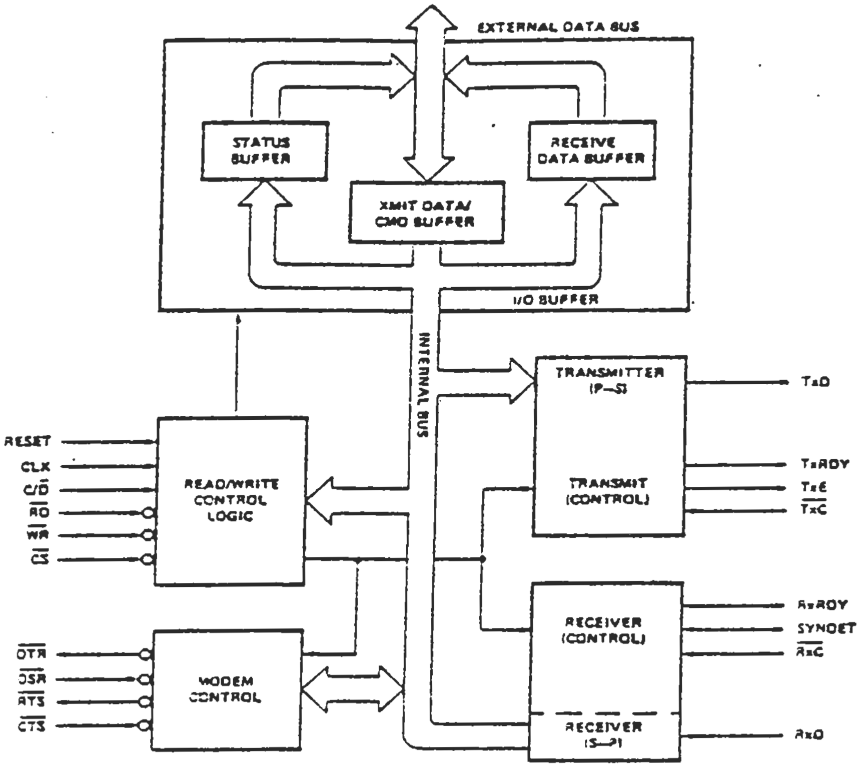


Figure 2. 8251 Block Diagram

CE	C/$\overline{D}$	$\overline{READ}$	$\overline{WRITE}$	Function
0	0	0	1	CPU Reads Data from USART
0	1	0	1	CPU Reads Status from USART
0	0	1	0	CPU Writes Data to USART
0	1	1	0	CPU Writes Command to USART
1	X	X	X	USART Bus Floating (NO-OP)

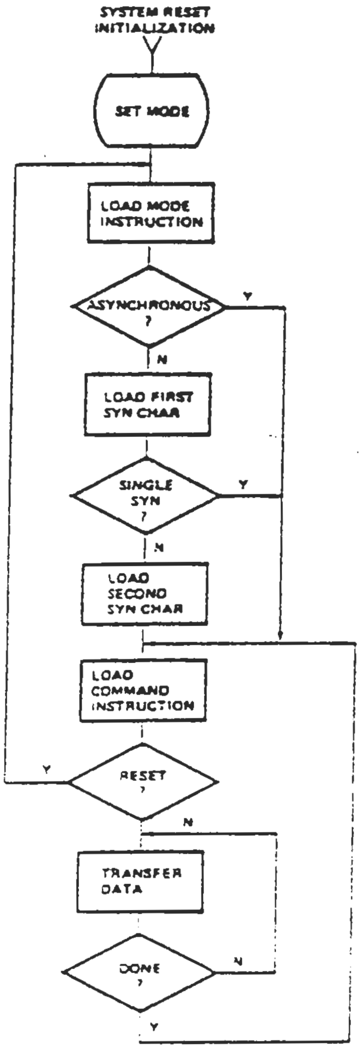


Figure 4. Initialization Flowchart

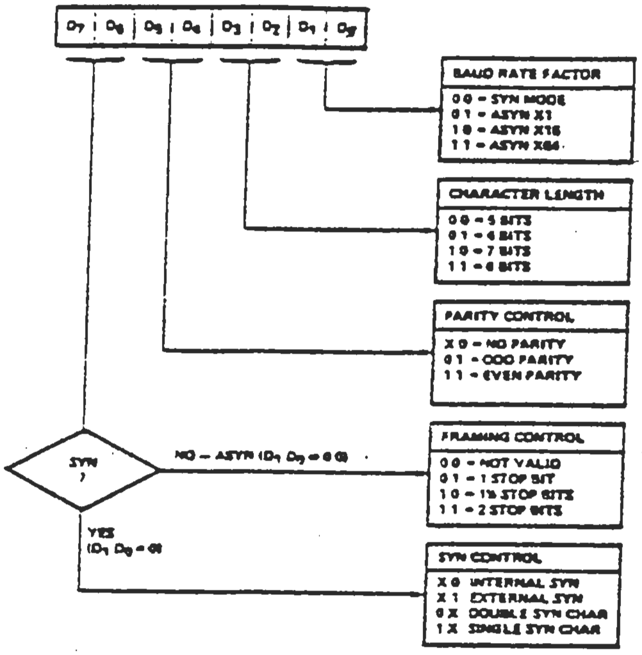


Figure 5. Mode Instruction Format

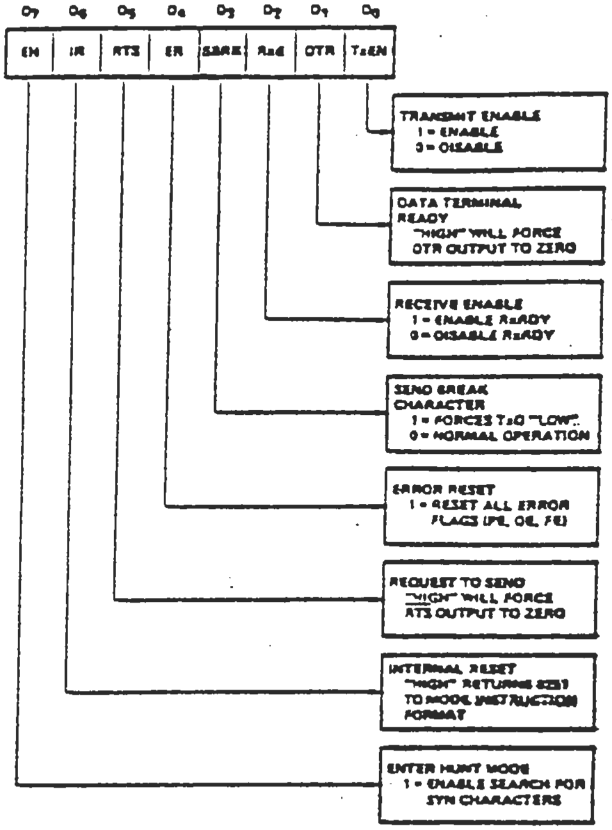
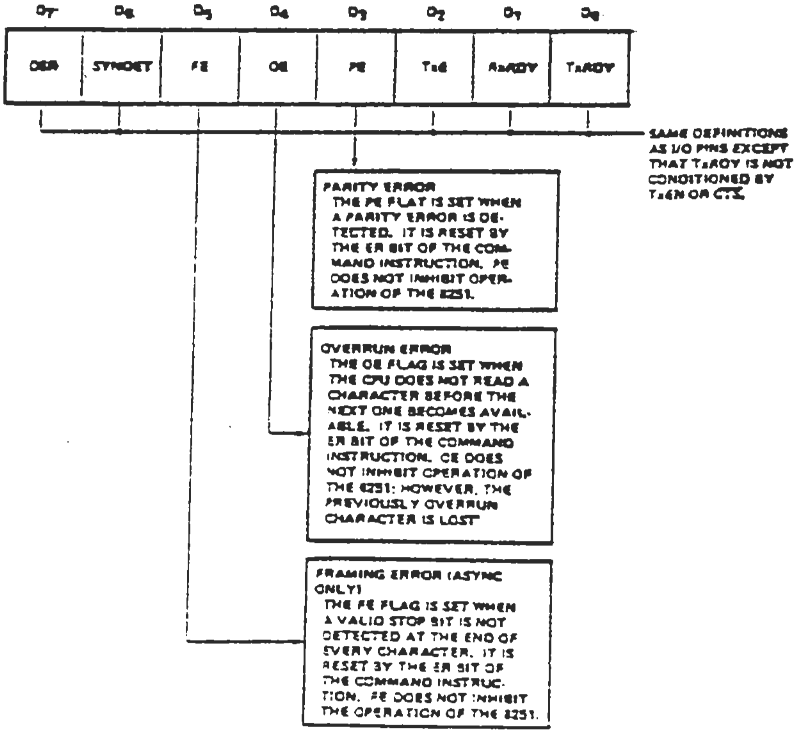


Figure 6. Command Instruction Format



D7 D6 D5 D4 D3 D2 D1 D0
DSR SYNDET FE OE PE TxE RxRDY TxRDY
SAME DEFINITIONS AS I/O PINS EXCEPT THAT TxRDY IS NOT CONDITIONED BY TxEN OR CTS.
PARITY ERROR
THE PE FLAT IS SET WHEN A PARITY ERROR IS DETECTED. IT IS RESET BY THE ER BIT OF THE COMMAND INSTRUCTION. PE DOES NOT INHIBIT OPERATION OF THE 8251.
OVERRUN ERROR
THE OE FLAG IS SET WHEN THE CPU DOES NOT READ A CHARACTER BEFORE THE NEXT ONE BECOMES AVAILABLE. IT IS RESET BY THE ER BIT OF THE COMMAND INSTRUCTION. OE DOES NOT INHIBIT OPERATION OF THE 8251; HOWEVER, THE PREVIOUSLY OVERRUN CHARACTER IS LOST.
FRAMING ERROR (ASYNC ONLY)
THE FE FLAG IS SET WHEN A VALID STOP BIT IS NOT DETECTED AT THE END OF EVERY CHARACTER. IT IS RESET BY THE ER BIT OF THE COMMAND INSTRUCTION. FE DOES NOT INHIBIT THE OPERATION OF THE 8251.

Figure 7. Status Register Format

compared to a register holding the SYN character (program loaded). If the two registers are now equal, the USART shifts in another bit and repeats the comparison. When the registers compare as equal, the USART ends the HUNT mode and raises the SYNDET line to indicate that it has achieved synchronization. If the USART has been programmed to operate with two SYN characters the process is as described above, except that two contiguous characters from the line must compare to the two stores SYN characters before synchronization is declared. Parity is not checked. The USART enters the HUNT mode when it is initialized into the synchronous mode or when it is commanded to do so by the command instruction. Before the receiver is operated, it must be enabled by the RxE bit (D_2) of the command instructions. If this bit is not set the receiver will not assert the RxRDY bit.

TRANSMITTER

The transmitter accepts parallel data from the processor, adds the appropriate framing information, serializes it, and transmits it on the TxD pin. In the asynchronous mode the transmitter always adds a START bit; depending on how the unit is programmed, it also adds an optional even or odd parity bit, and either 1, 1½ or 2 STOP bits. In the synchronous mode no extra bits (other than parity, if enable) are generated by the transmitter unless the computer fails to send a character to the USART. If the USART is ready to transmit a character and a new character has not been supplied by the computer, the USART will transmit a SYN character. This is necessary since synchronous communications, unlike asynchronous communications, does not allow gaps between characters. If the USART is operating in the dual SYN mode, both SYN characters will be transmitted before the message can be resumed. The USART will not generate SYN characters until the software has supplied at least one character; i.e., the USART will fill 'holes' in the transmission but will not initiate transmission itself. The SYN characters which are to be transmitted by the USART are specified by the software during the initialization procedure. In either the synchronous or asynchronous modes, transmission is inhibited until TxEnable and the $\overline{\text{CTS}}$ input are asserted.

An additional feature of the transmitter is the ability to transmit a BREAK. A BREAK is a period of continuous SPACE on the communication line and is used in full fuplex communication to interrupt the transmitting terminal. The USART will transmit a BREAK condition as long as bit 3 (SBRK) of the command register is set.

MODEM CONTROL

The modem control section provides for the generation of $\overline{\text{RTS}}$ and the reception of $\overline{\text{CTS}}$. In addition, a general purpose output and a general purpose input are provided. The output is labeled $\overline{\text{DTR}}$ and the input is labeled $\overline{\text{DSR}}$. $\overline{\text{DTR}}$ can be asserted by setting bit 2 of the command instruction; $\overline{\text{DSR}}$ can be sensed as bit 7 of the status register. Although the USART itself attaches no special significance to these signals, DTR (Data Terminal Ready) is normally assigned to the modem, indicating that the terminal is ready to communicate and DSR (Data Set Ready) is a signal from the modem indicating that it is ready for communications.

I/O CONTROL

The Read/Write Control Logic decodes control signals on the 8080 control bus into signals which gate data on and off the USART's internal bus and controls the external I/O bus (DB_0 - DB_7). The receiver and transmitter buffers are located at port #0 while the status and command buffers are port #1. The I/O buffer contains the STATUS buffer, the RECEIVE DATA buffer and the XMIT DATA/CMD buffer as shown in Figure 2. Note that although there are two registers which store data for transfer to the CPU (STATUS and RECEIVE DATA), there is only one register which stores data being transferred to the USART. The sharing of the input register for both transmit data and command makes it important to ensure that the USART does not have data stored in this register before sending a command to the device. The TxRDY signal can be monitored to accomplish this. Neither data nor commands should be transferred to the USART if TxRDY is low. Failure to perform this check can result in erroneous data being transmitted.

MODE SELECTION

The USART is capable of operating in a number of modes (e.g., synchronous or asynchronous). In order to keep the hardware as flexible as possible (both at the chip and end product levels), these operating modes are selected via a series of control outputs to the USART. These mode control outputs must occur between the time the USART is reset and the time it is utilized for data transfer. Since the USART needs this information to structure its internal logic it is essential to complete the initialization before any attempts are made at data transfer (including reading status).

A flowchart of the initialization process appears in Figure 4. The first operation which must occur following a reset is the loading of the mode control register. The mode control register is loaded by the first control output following a reset. The format of the mode control instruction is shown in Figure 5. The instruction can be considered as four 2-bit fields. The first

2-bit field (D_1D_0) determines whether the USART is to operate in the synchronous (00) or asynchronous mode. In the asynchronous mode this field also controls the clock scaling factor. As an example, if D_1 and D_0 are both ones, the $\overline{RxC}$ and $\overline{TxC}$ will be divided by 64 to establish the baud rate. The second field, D_3 - D_2, determines the number of data bits in the character and the third, D_5 - D_4, controls parity generation. Note that the parity bit (if enabled) is added to the data bits and is not considered as part of them when setting up the character length. As an example, standard ASCII transmission, which is seven bits plus even parity would be specified as:

X X 1 1 1 0 X X

The last field, D_7 - D_6, has two meanings, depending on whether operation is to be in the synchronous or asynchronous mode. For the asynchronous mode (i.e., $D_1D_0 \neq 00$), it controls the number of STOP bits to be transmitted with the character. Since the receiver will always operate with only one STOP bit, D_7 and D_6 only control the transmitter. In the synchronous mode, (D_1D_0=00), this field controls the synchronizing process. Note that the choice of single or double SYN characters is independent of the choice of internal or external synchronization. This is because even though the receiver may operate with external synchronization logic, the transmitter must still know whether to send one or two SYN characters should the CPU fail to supply a character in time.

Following the loading of the mode instruction the appropriate SYN character (or characters) must be loaded if synchronous mode has been specified. The SYN character(s) are loaded by the same control output instruction used to load the mode instruction. The USART determines from the mode instruction whether no, one, or two SYN characters are required and uses the control output to load SYN characters until the required number are loaded.

At completion of the load of SYN characters (or after the mode instruction in the asynchronous mode), a command character is issued to the USART. The command instruction controls the operation of the USART within the basic framework established by the mode instruction. The format of the command instruction is shown in Figure 6. Note that if, as an example, the USART is waiting for a SYN character load and instead is issued an internal reset command, it will accept the command as an SYN character instead of resetting. This situation, which should only occur if two independent programs control the USART, can be avoided by outputting three all zero characters as commands before issuing the internal reset command. The USART indicates its state in a status register which can be read under program control. The format of the status register read is shown in Figure 7.

When operating the receiver it is important to realize that RxE (bit 2 of the command instruction) only inhibits the assertion of RxRDY; it does not inhibit the actual reception of characters. Because the receiver is constantly running, it is possible for it to contain extraneous data when it is enabled. To avoid problems this data should be read from the USART and discarded. The read should be done immediately following the setting of Receive Enable in the asynchronous mode, and following the setting of Enter Hunt in the synchronous mode. It is not necessary to wait for RxRDY before executing the dummy read.

USART INTERRUPTS

The SYNDET, TxRDY, and RxRDY flags will cause an interrupt if they are set. These three flags are ored together and applied to interrupt 3. This connection may be broken, if this interrupt is not used, by cutting trace "K" on the CPU card. Two adjacent pads are provided to reconnect the interrupt later, if desired.

When using the PolyMorphic Systems Monitor ROM the K jumper should be cut for monitor versions 2.Ø and 2.2 and connected for version 3.Ø.

USART ADDRESSING

The transmit and receive buffers are addressed as port Ø on the CPU card if it is set up for operation at Ø. The command and status buffers are located at port 1. If your CPU card is not setup for operation at Ø consult the following table.

SER/8 ADDRESSING

Address Jumper	ROM begins at	Data port	Command & Status Port	Baud Rate Generator Latch
J (factory set)	ØØØØ	Ø	1	4
T	8ØØØ	8Ø	81	84
S	EØØØ	EØ	E1	E4

BAUD RATE GENERATOR OPERATION

The baud rate generator may be accessed through port #4. The byte output to this port will be latched into the baud rate latch and determines the baud rate, device number, and ROM disable or enable. When power is applied to the CPU card or the front panel reset button is pushed, this latch is set to Ø. The command format is as follows:

D_7 D_6	D_5	D_4	D_3	$D_{\emptyset}$
Unused	ROM disable	Device #	Baud Rate	

BAUD RATE

The baud rate field may assume 1 of 16 values of Ø through F (base 16). 15 of these are valid baud rates, Ø disables clock generation. Note that the actual baud rate is determined by the USART mode (x1, x16, x64 clock). See Figure 8 for the available baud rates.

SER/8 Baud Rates

	USART mode	x1	x16	x64
Baud Rate Field				
Binary	Hex			
0001	1	800	50	12.5
0010	2	1200	75	18.75
0011	3	1760	110	27.5
0100	4	2152	134.5	33.62
0101	5	2400	150	37.5
0110	6	4800	300	75
0111	7	9600	600	150
1000	8	14400	900	225
1001	9	19200	1200	300
1010	A	28800	1800	450
1011	B	38400	2400	600
1100	C	57600	3600	900
1101	D	----	4800	1200
1110	E	----	7200	1800
1111	F	----	9600	2400

Figure 8.

DEVICE NUMBER

This bit selects the device to be connected to the USART. Two devices (Ø and 1) may share the USART on the CPU board. When a device is enable it sends data, receive clock, CTS and DSR to the USART through a tri-state buffer. Transmit data, clock, RTS and DTR are anded with the device select signal at the device. Device Ø is normally a cassette interface minicard and device 1 is normally a RS-232/current loop minicard. (Note that the 2 DIP sockets on the CPU do not determine the device number).

ROM DISABLE

Bit 5 of the BRG control word normally is not enabled. When enabled by connecting a jumper on the CPU card, it will disable the onboard ROM and RAM when true. This option should be used with caution as disabling the onboard ROM while executing the monitor routines may cause unpredictable results. (See application note on ROM disable option use).

APPENDIX A
PROGRAMMING HINTS

1. Output of a command to the USART destroys the integrity of a transmission in progress if timed incorrectly.

   Sending a command into the USART wll overwrite any character which is stored in the buffer waiting for transfer to the parallel-to-serial converter in the device. This can be avoided by sending a command if transmission is taking place. Due to theinternal structure of the USART, it is also possible to disturb the transmission if a command is sent while SYN character is being generated by the device. (The USART generates a SYN if the software fails to respond to TxRDY). If this occurrence is possible in a system, commands should be transferred only when a positive-going edge is detected on the TxRDY line).

2. RxE only acts as a mask to RxRDY; it does not control the operation of the receiver.

   When the receiver is enabled, it is possible for it to already contain one or two characters. These characters should be read and discarded when the RxE bit is first set. Because of these extraneous characters the proper sequence for gaining synchronization is as follows:
   1.Disable interrupts.

   2.Issue a command to enter hunt mode, clear errors, and enable the receiver (EH,ER,RxE=1).

   3.Read USART data (it is not necessary to check status).

   4.Enable interrupts.

The first RxRDY that occurs after the above sequence will indicate that the SYN character or characters have been detected and the next character has been assembled and isready to be read.

3. Loss of CTS or dropping TxEnable will immediately clamp the serial output line.

   TxEnable and RTS should remain asserted until the transmission is complete. Note that this implies that not only has the USART completed the transfer of all bits of the last character, but also that they have cleared the modem. A delay of 1 msec following a proper occurence of TxEmpty is usually sufficient (see Item 4). An additional problem can occur in the synchronous mode because the loss of TxEnable clamps the data in at a SPACE instead of the normal MARK. This problem, which does not occur in the asynchronous mode, can be corrected by an external gate combining RTS and the serial output data.

4. Extraneous transitions can occur on TxEmpty while data (including USART generated SYNs) is transferred to the parallel-to-serial converter,

   This situation can be avoided by ensuring that TxEmpty occurs during several consecutive status reads before assuming that the transmitter is truly in the empty state.

5. A BREAK (i.e., long space) detected by the receiver results in a string of characters which have framing errors.

   If reception is to be continued after a BREAK, care must be taken to ensure that valid data is being received; special care must be taken with the last character perceived during a BREAK, since its value, including any framing error associated with it, is indeterminate.

Interfacing to the POLY-88 Bus

Data Bus - Data transfer in the POLY-88 occurs over two unidirectional data busses - the Data In bus, DIØ-7 (device to CPU transfer) and the Data Out bus, DØ1-7 (CPU to device transfer). Both busses are 8 bits wide. The Data Out bus is tri-state and will drive 30 TTL loads or 120 low-power schottky TTL (LSTTL) loads. The Data In bus present 1 LSTTL load. D7 is the most significant bit during arithmetic operations. Data is presented on the bus uncomplemented.

Address Bus - The Address Bus, AØ - A15, is 16 bits wide and is also tri-state for DMA or multiprocessing applications. It also will drive 30 TTL or 120 LSTTL loads. During memory transfers a 16 bit memory address appears on this bus. A15 is the most significant address bit. During I/O transfers two identical 8 bit addresses appear on the bus. A15 and A7 are the most significant address bits. Generally the lower 8-bits (AØ - 7) are used to address I/O devices.

Interrupt Bus - The Interrupt Bus (VIØ - VI7) consists of eight active low interrupt request lines. VI7 is the interrupt with the highest priority and VIØ has the lowest priority. Each of these lines present 1 TTL load to the bus and each is pulled up by a 2200 ohm resistor to +5 volts to ensure unused interrupts are inactive. An interrupt request should remain low until services by the CPU.

Status Bus - These 6 lines indicate the status of the CPU (i.e.- what type of cycles it is running). SINTA goes high during and interrupt acknowledge cycle; SMEMR, when high, signals a memory read cycle; SIN and SOUT, respectively, indicate input and output data transfers. SWO goes low during output or memory write cycles, and HLTA is active (high) only when the CPU is halted. Note that there is not a separate status line for a memory write cycle. This may be generated by the logic $SWO \cdot \overline{SOUT}$. All status lines, except HLTA, are tri-state and capable of driving 30 TTL loads. HLTA is an open collector output with a resistive pulley of 1000Ω to +5 volts.

Clocks - The two 8080 CPU clocks Ø1 and Ø2 are buffered and brought out to the bus. Both clocks are active high.

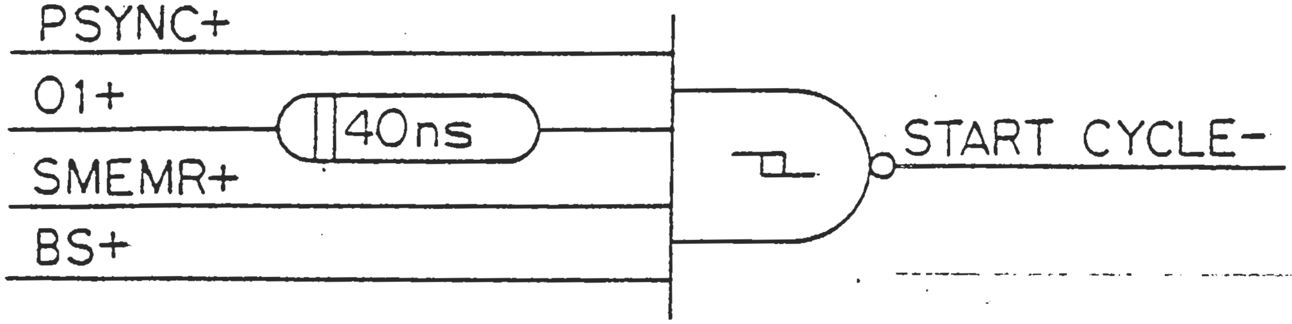
Control Bus and Data Strobes - Two lines are provided for cold starting the CPU. The PRESET line (active low) causes the program counter to be reset to zero, and when release (high) starts execution from that point with interrupts disabled. PRESET may be generated by a mechanical switch closure as an RC timing network and pullups are provided on the CPU/8 cards. POC is an active low signal that is asserted whenever PRESET is active. It is open-collector with a 2.2K pullup to +5 volts and is normally used to reset peripheral controllers when power is applied to the system or during a reset.
XRDY, PRDY, and BGNT are all anded together and applied to the 8080 CPU as the READY signal. When any of these are low the processor will enter a wait state the next time it tries to access the bus and will remain in a wait state until XRDY PRDY, and BGNT are all high. These three inputs are pulled high through 2200Ω resistors to +5 volts to ensure they are active when unused. The PRDY line is to be used by memory and peripheral controllers to indicate that a transfer cannot be completed within the 500 nanosecond CPU cycle, and will extend this cycle by adding wait cycles, until PRDY is high.

BGNT and XRDY are to be used only by the bus controller card. BGNT, when taken low, will also disable all tri-state bus drivers on the CPU/8 card. The data strobes PDBIN and PWR are processor data bus in and processor write, respectively. PDBIN is active high and PWR is active low. When PDBIN is active data for a transfer to the CPU should be gated onto the data in bus. When PWR is active, valid data is present on the data out bus for a transfer to a peripheral device on memory. The PSYNC signal is asserted (active high) at the beginning of every memory or I/O cycle. During this time, the processor status word is being sent to the status latch. Shortly after the rising edge of Ø1 during PSYNC the status is available. A delay of 40 ns after the positive edge of Ø1 is satisfactory. The memory or I/O address (AØ - A15) is stable shortly after the rising edge of PSYNC (see timing diagram). An additional strobe, PMWR or MWRITE, is provided on the bus. This is an active high signal that is the logical end of PWR+ and SOUT-. It is to be used as the write strobe for memory transfers.

Using Static Devices on the POLY-88

Bus -- Devices such as static ROM or RAM or I/O parts are easy to interface to the Poly-88 bus.Addresses and chip selects may be decoded directly from the address bus and applied to the memory or I/O devices. PDBIN and the status of the operation (SINP or SMEMR) should be used to gate data onto the bus. When writing MWRITE or PWR·SOUT should be used as the write strobe. If data is to be gated onto an oncard bus, $\overline{\text{SYNC}}$·WO should be used. Otherwise the DO bus should be buffered and applied continuously. When designing an interface to the bus all data strobes should be applied to Schmidt-trigger inputs for noise immunity. See Figure X for an example.

Additional interfacing for dynamic or clocked devices - When interfacing to dynamic RAM a signal is needed to indicate the start if an access cycle. This may be produced by anding together Ø1, SYNC, the appropriate status bit and a board select (BS) signal. BS indicates that a valid address has been decoded. Shown below is a circuit for decoding the start of a memory read cycle.



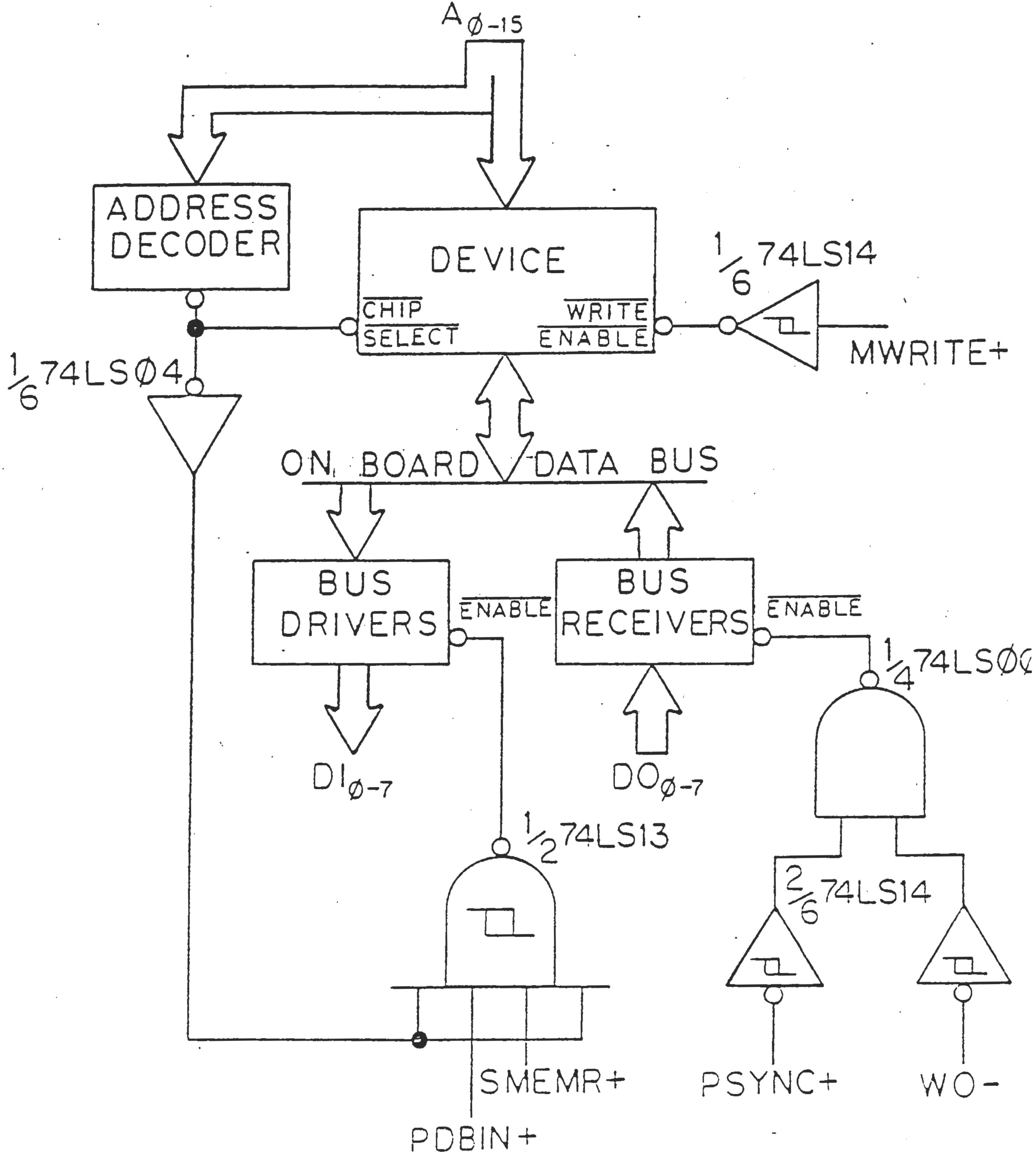
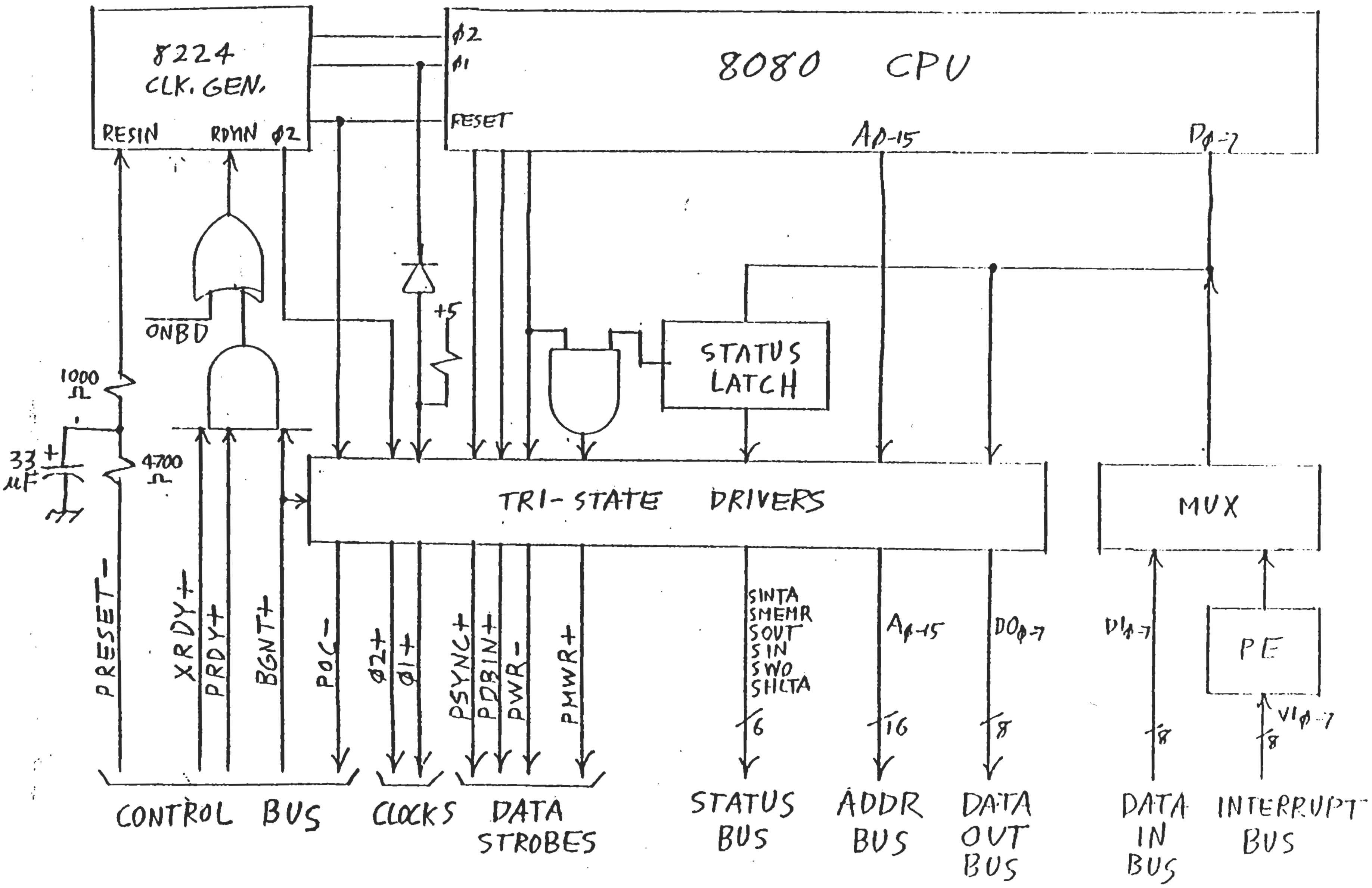

A$_{\emptyset-15}$
ADDRESS DECODER
DEVICE
CHIP SELECT
WRITE ENABLE
1/6 74LS14
MWRITE+
1/6 74LS$\emptyset$4
ON BOARD DATA BUS
BUS DRIVERS
ENABLE
BUS RECEIVERS
ENABLE
1/4 74LS$\emptyset$0
DI$_{\emptyset-7}$
DO$_{\emptyset-7}$
1/2 74LS13
2/6 74LS14
SMEMR+
PDBIN+
PSYNC+
WO-

FIG X

CPU/8 BUS INTERFACE



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